Power Modeling for Arbitrary RTL Designs

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For this project, we will develop power models for any novel RTL designs for a specific technology to quickly obtain the power estimates from FPGA simulations. Power estimation using CAD tools, i.e. gate-level simulation with PrimeTimePX, is very accurate but extremely slow. Micro-architectural analytic power modeling [1], [2] with micro-architectural cycle-level software simulators [3], [4] is very popular for computer architects because it is easy to use and faster than CAD tools. However, this methodology still much slower than real hardware, so it is practically impossible to obtain the power estimates of a full program execution. Moreover, it always imposes validation issues for novel hardware designs, and thus, may report misleading power estimates without rigorous validation. Kim et al. [5] show that we can accelerate power estimation using random samples from FPGA simulation, but power estimates are not available until sample replays on gate-level simulation are done, preventing online power analysis during FPGA simulation.

Specifically, important signals in a random RTL design will be selected by circuit topology analysis and/or the training data, and the power model in terms of the selected signals will be trained with the power data from micro-benchmarks or realistic long applications when available. We currently do not have an idea how to select the signals and train the model, but we will figure it out using the knowledge covered in this class. Once the important signals and the power models are figured out, the RTL design is also transformed and instrumented to collect signal activities from FPGA simulation. Power estimates can be easily obtained in the middle of the execution by stopping the simulation and reading out the activities counters. The simulation can be easily resumed because the RTL design is FAME-1 transformed. [5] The power model will also be validated using Strober. [5]

References

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