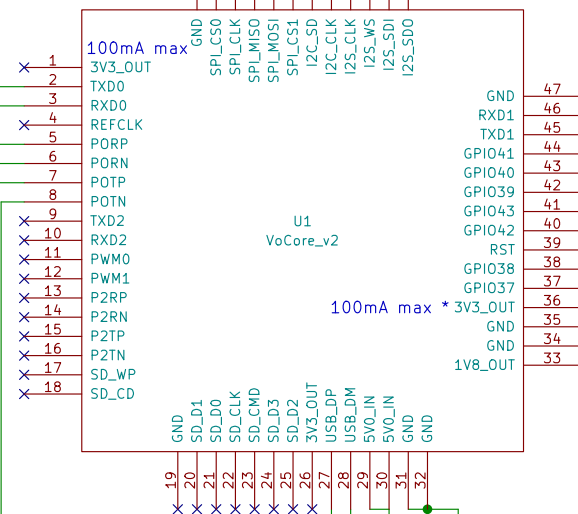
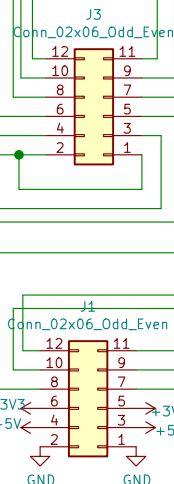
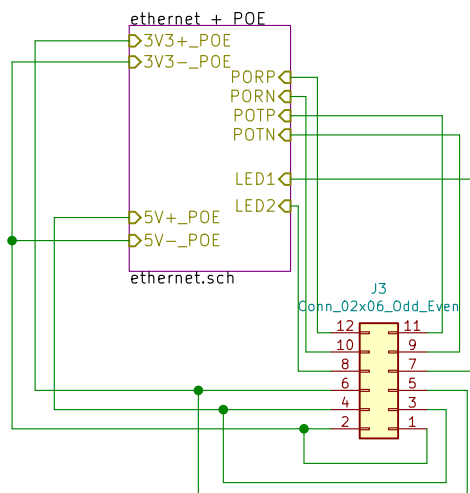


XXX: Add decoupling caps on power rails as shown in laf0rge minipcie schematic:

<https://osmocom.org/projects/mpcie-breakout/wiki>

XXX: Review reset state for those two lines. pull-up/pull-down accordingly.



PINS 39, 40, 41 can be used as ETH PHY LED GPIOs according to Mediatek 7688AN datasheet



XXX: PMOD expanded SPI (type 2A) should offer the highest flexibility?

XXX: Implement 3.3V and 5V optional switch according to PMOD spec?

MiniPCle breakout (n-fuse and RAK833 LoRa gateways)
... perhaps other devices too

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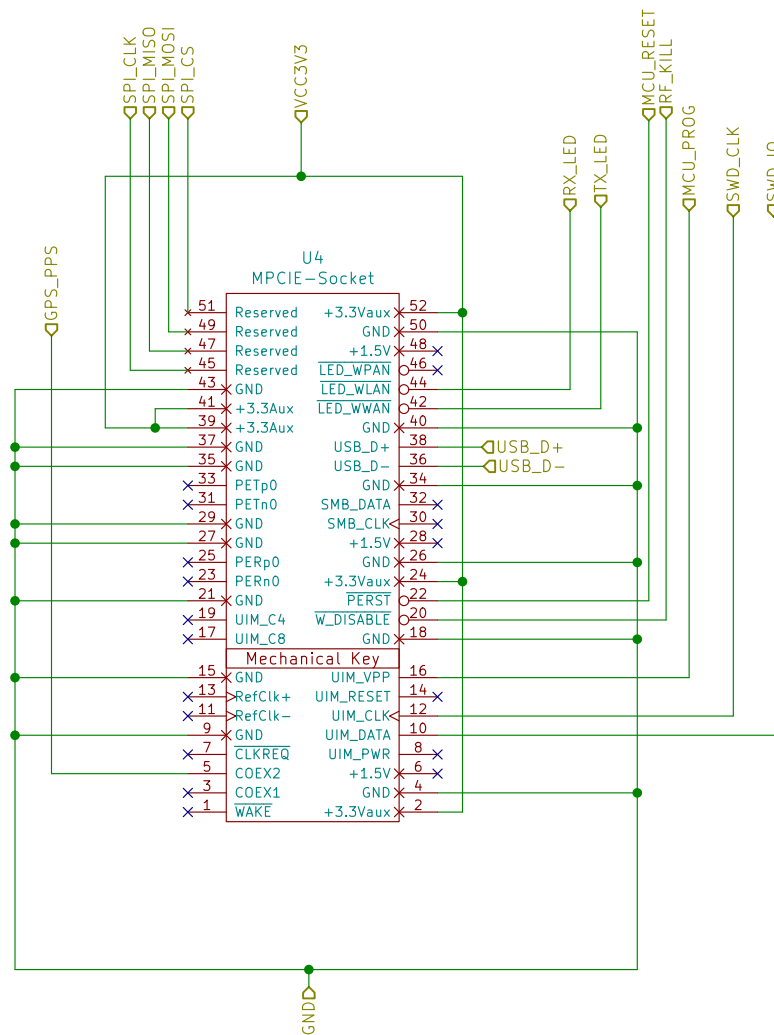
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Those pins are reserved on the mpcie spec
RAK833 LoRa GW uses them for SPI, perhaps
others like n-fuse will use the same in the future?



Pins mapped according to n-fuse datasheet:
<https://www.n-fuse.co/products/lrwcx/lrwcx-mpcie-datasheet.pdf>

MiniPICe (reserved) SPI pins according to RAK833 datasheet.

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