



# SGM58031

## Ultra-Small, Low-Power, 16-Bit

### Analog-to-Digital Converter with Internal Reference

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## GENERAL DESCRIPTION

The SGM58031 is precision analog-to-digital converter (ADC) with 16 bits of resolution. The SGM58031 is designed with precision, low power, and ease of implementation. The SGM58031 features an on-chip reference and oscillator. Data are transferred via an I<sup>2</sup>C-compatible serial interface; four I<sup>2</sup>C slave addresses can be selected. The SGM58031 operates from a single power supply ranging from 3V to 5.5V.

The SGM58031 can perform conversions at rates up to 960 samples per second (SPS). An on-chip PGA is available on the SGM58031 that offers input ranges from the supply to as low as  $\pm 256\text{mV}$ , allowing both large and small signals to be measured with high resolution. The SGM58031 also features an input multiplexer (MUX) that provides two differential or four single-ended inputs.

The SGM58031 operates either in continuous conversion mode or a single-shot mode that automatically powers down after a conversion and greatly reduces current consumption during idle periods.

The SGM58031 is available in Green MSOP-10 and TDFN-3 $\times$ 3-10L packages and it is specified from -40°C to +125°C.

## FEATURES

- **Wide Power Supply Range: 3V to 5.5V**
  - ◆ **I<sup>2</sup>C Bus Voltage: 3V to 5.5V**
- **Low Current Consumption:**
  - Continuous Mode: 255 $\mu$ A (TYP)**
  - Power-Down Mode: 0.8 $\mu$ A (TYP)**
- **Programmable Data Rate: 6.25SPS to 960SPS**
- **Internal Low-Drift Voltage Reference**
- **Internal Oscillator**
- **Internal PGA**
- **I<sup>2</sup>C Interface: Pin-Selectable Addresses**
- **Four Single-Ended or Two Differential Inputs**
- **Programmable Comparator**
- **Available in Green MSOP-10 and TDFN-3 $\times$ 3-10L Packages**

## APPLICATIONS

Portable Instrumentation  
Consumer Goods  
Battery Monitoring  
Temperature Measurement  
Factory Automation and Process Controls

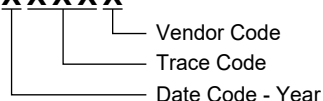
## PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM58031	MSOP-10	-40°C to +125°C	SGM58031XMS10G/TR	SGM58031 XMS10 XXXXX	Tape and Reel, 4000
	TDFN-3x3-10L	-40°C to +125°C	SGM58031XTD10G/TR	SGM 58031D XXXXX	Tape and Reel, 4000

## MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

XXXXX



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to GND .....	-0.3V to 5.5V
Analog Input Voltage to GND.....	-0.3V to 5.5V
SDA, SCL, ADDR, ALERT/RDY Voltage to GND .....	-0.3V to 5.5V
Analog Input Current (Momentary) .....	100mA
Analog Input Current (Continuous) .....	10mA
Junction Temperature .....	+150°C
Storage Temperature Range .....	-65°C to +150°C
Lead Temperature (Soldering, 10s) .....	+260°C
ESD Susceptibility	
HBM.....	4000V
CDM .....	1000V

## RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range .....	-40°C to +125°C
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## OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

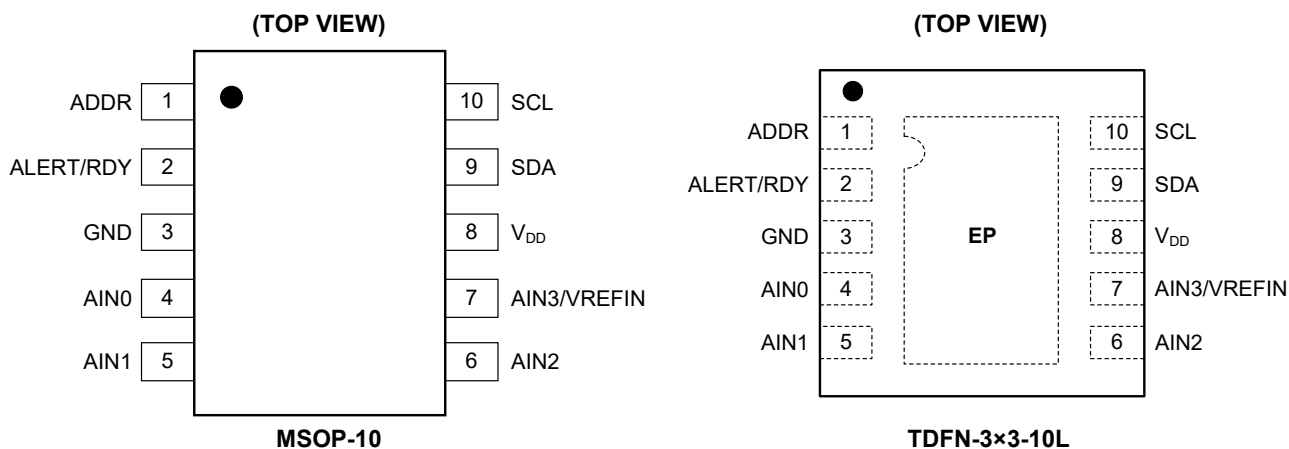
## ESD SENSITIVITY CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

## PIN CONFIGURATIONS



## PIN DESCRIPTION

PIN		NAME	TYPE	FUNCTION
MSOP-10	TDFN-3x3-10L			
1	1	ADDR	Digital Input	I <sup>2</sup> C Slave Address Select.
2	2	ALERT/RDY	Digital Output	Digital Comparator Output or Conversion Ready.
3	3	GND	Ground	Ground.
4	4	AIN0	Analog Input	Positive Input of Differential Channel 1 or Input of Single-Ended Channel 1.
5	5	AIN1	Analog Input	Negative Input of Differential Channel 1 or Input of Single-Ended Channel 2.
6	6	AIN2	Analog Input	Positive Input of Differential Channel 2 or Input of Single-Ended Channel 3.
7	7	AIN3/VREFIN	Analog Input	Negative Input of Differential Channel 2, or Input of Single-Ended Channel 4, or External Reference Input.
8	8	V <sub>DD</sub>	Power	3V to 5.5V Power Supply.
9	9	SDA	Digital I/O	Serial Data. Transmits and receives data.
10	10	SCL	Digital Input	Serial Clock Input. Clocks data on SDA.
–	Exposed Pad	EP	–	Exposed pad should be soldered to PCB board and connected to GND.

# Ultra-Small, Low-Power, 16-Bit

## Analog-to-Digital Converter with Internal Reference

### SGM58031

## ELECTRICAL CHARACTERISTICS

( $V_{DD} = 3.3V$ , Full-Scale (FS) =  $\pm 2.048V$ , maximum and minimum specifications apply from  $T_A = -40^\circ C$  to  $+125^\circ C$ , typical values are at  $T_A = +25^\circ C$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Input						
Full-Scale Input Voltage <sup>(1)</sup>		V <sub>IN</sub> = (A <sub>INP</sub> ) - (A <sub>INN</sub> )		±4.096/PGA		V
Analog Input Voltage		A <sub>INP</sub> or A <sub>INN</sub> to GND	GND		V <sub>DD</sub>	V
Differential Input Impedance				See Table 2		
System Performance						
Resolution		No missing codes	16			Bits
Data Rate	DR			See Table 6		SPS
Data Rate Variation		All data rates	-6		6	%
Output Noise			See Table 7 and Table 8			
Integral Nonlinearity	INL	DR = 8SPS, FS = ±2.048V, best fit <sup>(2)</sup>		1	4	LSB
Offset Error		FS = ±2.048V, differential inputs		1	5	LSB
		FS = ±2.048V, single-ended inputs		2	8.5	
Offset Drift		FS = ±2.048V		0.005	0.06	LSB/°C
Offset Power-Supply Rejection		FS = ±2.048V		1.2		LSB/V
Gain Error <sup>(3)</sup>		FS = ±2.048V at +25°C		0.03	0.3	%
Gain Drift <sup>(4)</sup>		FS = ±0.256V		30		ppm/°C
		FS = ±2.048V		30	70	
		FS = ±6.144V <sup>(1)</sup>		30		
Gain Power-Supply Rejection				50	200	ppm/V
PGA Gain Match <sup>(3)</sup>		Match between any two PGA gains		0.1	0.28	%
Gain Match		Match between any two inputs		0.01	0.08	%
Offset Match		Match between any two gains		1	8.5	LSB
50/60Hz Rejection		FS = ±2.048V		95		dB
Channel-to-Channel Crosstalk		At DC and FS = ±2.048V, differential or single-ended inputs adjacent channels		90		dB
Common-Mode Rejection Ratio	CMRR	At DC and FS = ±0.256V		110		dB
		At DC and FS = ±2.048V		110		
		At DC and FS = ±6.144V <sup>(1)</sup>		110		
Internal Clock						
Frequency			386	410	434	kHz

### NOTES:

1. This parameter expresses the full-scale range of the ADC scaling. In no event should more than  $V_{DD} + 0.3V$  be applied to this device.
2. 99% of full-scale.
3. Includes all errors from on-chip PGA and reference.
4. Gain temperature drift is defined as the maximum change of gain error measured over the specified temperature range. The gain error drift is calculated using the box method, as described by Equation: Gain Error Drift =  $(GE_{MAX} - GE_{MIN}) / (T_{MAX} - T_{MIN})$  where:
  - $GE_{MAX}$  and  $GE_{MIN}$  are the maximum and minimum gain errors, respectively.
  - $T_{MAX}$  and  $T_{MIN}$  are the maximum and minimum temperatures, respectively, over the temperature range  $-40^\circ C$  to  $+125^\circ C$ .

**ELECTRICAL CHARACTERISTICS (continued)**

( $V_{DD} = 3.3V$ , Full-Scale (FS) =  $\pm 2.048V$ , maximum and minimum specifications apply from  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ , typical values are at  $T_A = +25^{\circ}C$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Reference</b>						
Internal Reference				2.048		V
External Reference			0.5		2.5	V
External Reference Input Current		$V_{REFIN} = 2.5V$ , continuous mode		0.45		$\mu A$
<b>Digital Input/Output</b>						
High Input Voltage <sup>(5)</sup>	$V_{IH}$		$0.7 \times V_{BUS}$			V
Low Input Voltage <sup>(5)</sup>	$V_{IL}$				$0.3 \times V_{BUS}$	V
Low Output Voltage	$V_{OL}$	$I_{OL} = 3mA$		0.07	0.4	V
High Input Leakage Current <sup>(6)</sup>	$I_{IH}$	$V_{IH} = 5.5V$		0.1	1	$\mu A$
Low Input Leakage Current <sup>(6)</sup>	$I_{IL}$	$V_{IL} = GND$		0.1	1	$\mu A$
<b>Power-Supply Requirements</b>						
Power-Supply Voltage	$V_{DD}$		3		5.5	V
Supply Current	$I_{DD}$	$V_{DD} = 5.5V$ , power-down current at $+25^{\circ}C$ <sup>(7)</sup>		0.8	1	$\mu A$
		$V_{DD} = 5.5V$ , power-down current up to $+125^{\circ}C$ <sup>(7)</sup>		1.8	3.8	
		$V_{DD} = 5.5V$ , operating current at $+25^{\circ}C$		255	320	
		$V_{DD} = 5.5V$ , operating current up to $+125^{\circ}C$		270	340	
Power Dissipation	$P_D$	$V_{DD} = 5V$		1.05		mW
		$V_{DD} = 3.3V$		0.6		

**NOTES:**

5. There are 2 scenarios:  $V_{DD} = 5V$ ,  $V_{BUS}$  can be 3V to 5V;  $V_{DD} = 3.3V$ ,  $V_{BUS}$  should be 3.3V. Note that  $V_{BUS} = 3V$  may cause leakage in some extreme conditions, and it's better to make it higher than 3.1V. For  $V_{BUS} = V_{DD}$ ,  $V_{IL}/V_{IH} = 30\%/70\%$  of  $V_{BUS}$ . For  $V_{BUS} = 3.3V$  and  $V_{DD} = 5V$ ,  $V_{IL}/V_{IH} = 20\%/80\%$  of  $V_{BUS}$ .

6. Meet the "loss of  $V_{DD}$ " requirement of  $I^2C$  fast mode. When  $V_{DD}$  is lost, the leakage drawn from the pin is controlled.

7. Power-down current increases to  $2.3\mu A$  at  $+25^{\circ}C$  and  $3.5\mu A$  at  $+125^{\circ}C$  when Config1 BUS\_FLEX is set to '1'.

## TIMING REQUIREMENTS

Table 1. I<sup>2</sup>C Timing Definitions

PARAMETER	SYMBOL	STANDARD MODE		FAST MODE		HIGH-SPEED MODE		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
SCL Operating Frequency	$f_{SCL}$	0.01	0.1	0.01	0.4	0.01	3.4	MHz
Bus Free Time between START and STOP Condition	$t_{BUF}$	4700		600		160		ns
Hold Time after Repeated START Condition. After this period, the first clock is generated.	$t_{HDSTA}$	4000		600		160		ns
Repeated START Condition Setup Time	$t_{SUSTA}$	4700		600		160		ns
Stop Condition Setup Time	$t_{SUSTO}$	4000		600		160		ns
Data Hold Time	$t_{HDDAT}$	0		0		0		ns
Data Setup Time	$t_{SUDAT}$	250		100		10		ns
SCL Clock Low Period	$t_{LOW}$	4700		1300		160		ns
SCL Clock High Period	$t_{HIGH}$	4000		600		60		ns
Clock/Data Fall Time	$t_F$		300		300		160	ns
Clock/Data Rise Time	$t_R$		1000		300		160	ns

Note that  $t_F$  (MIN) for SDA output is 20ns for normal/fast mode and 10ns for high-speed mode. Glitch filter capability is 50ns for normal/fast mode and 10ns for high-speed mode.

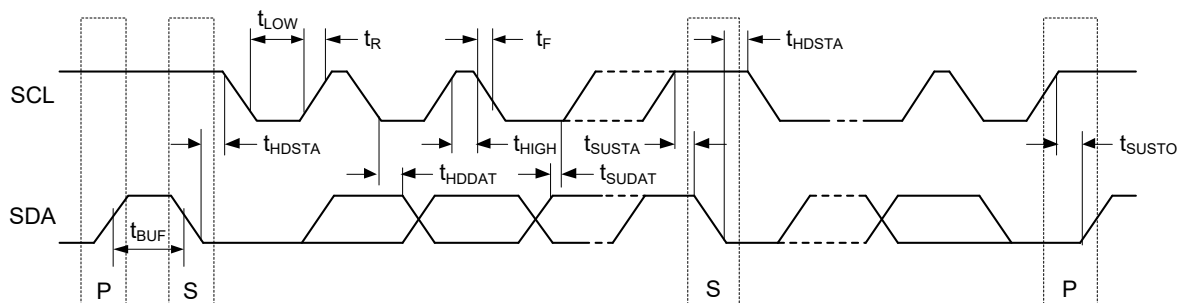
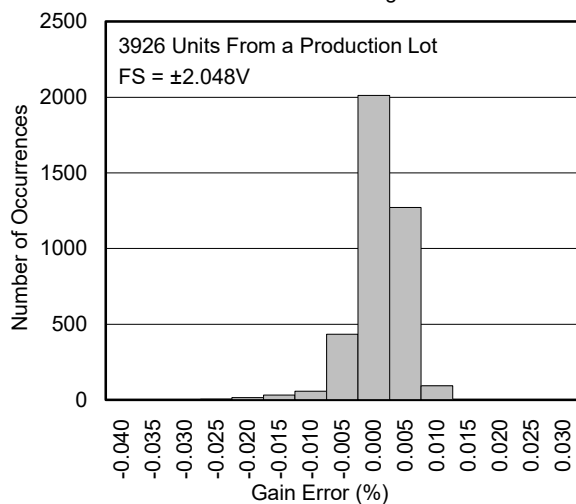


Figure 1. I<sup>2</sup>C Timing Diagram

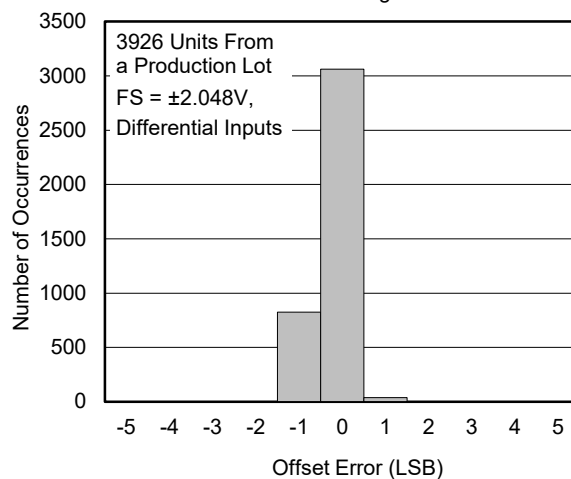
## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = +25^\circ\text{C}$ ,  $V_{DD} = 3.3\text{V}$ , Data Rate = 200SPS and Full-Scale (FS) =  $\pm 2.048\text{V}$ , unless otherwise noted.

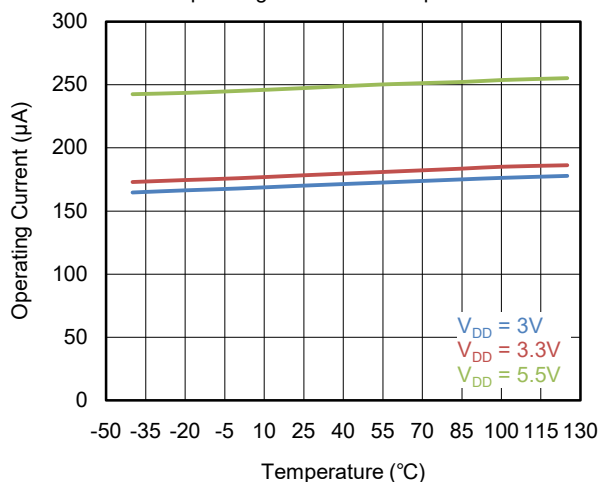
Gain Error Histogram



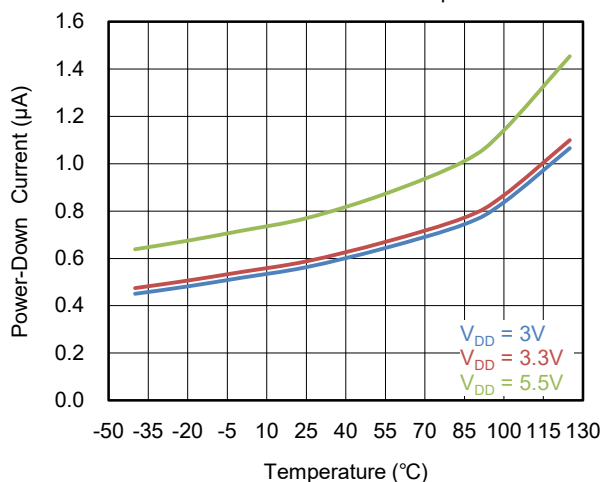
Offset Error Histogram



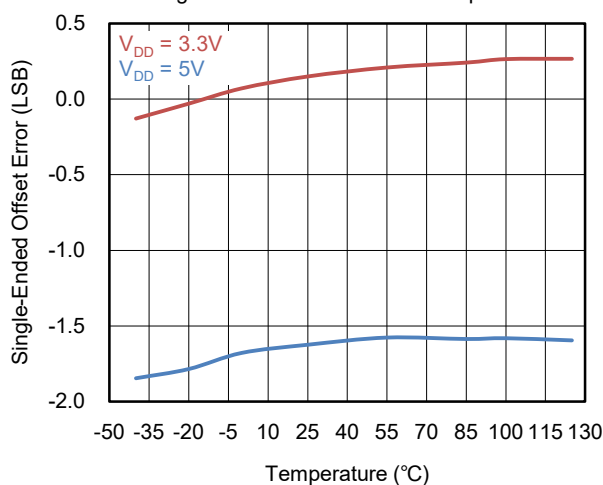
Operating Current vs. Temperature



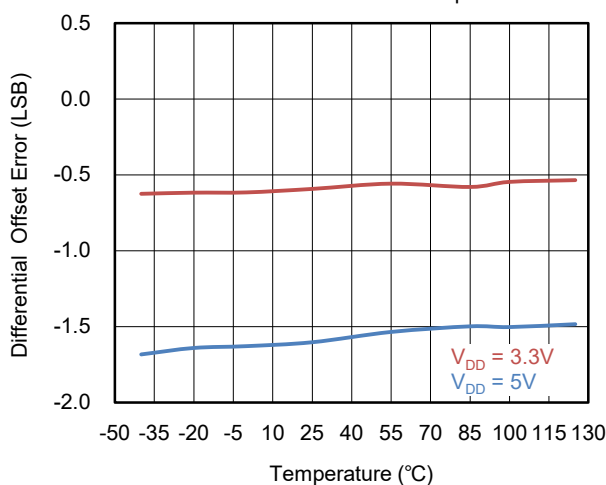
Power-Down Current vs. Temperature



Single-Ended Offset Error vs. Temperature

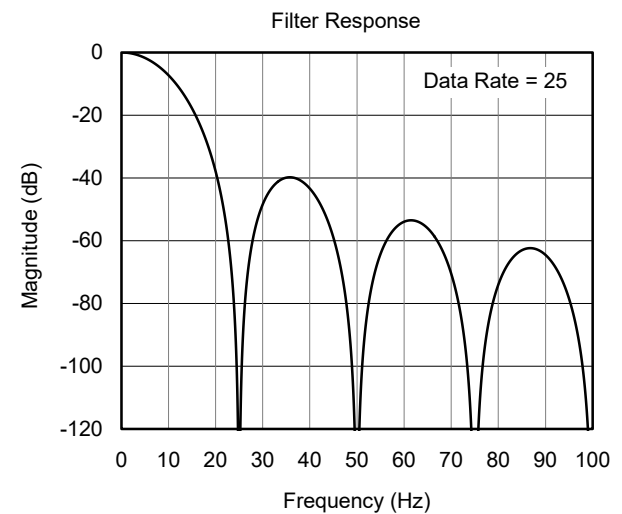
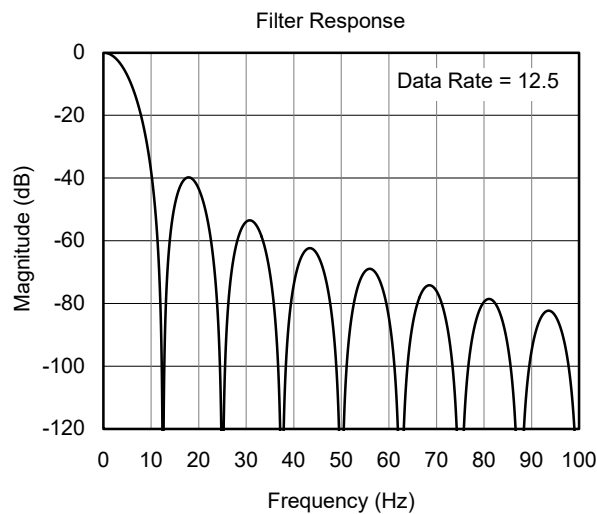
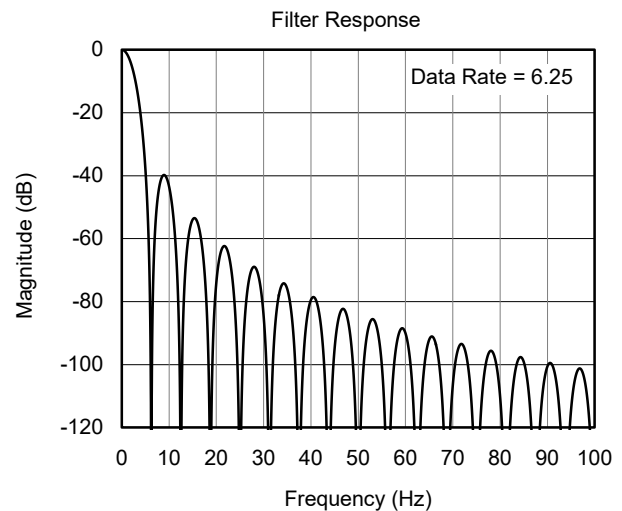
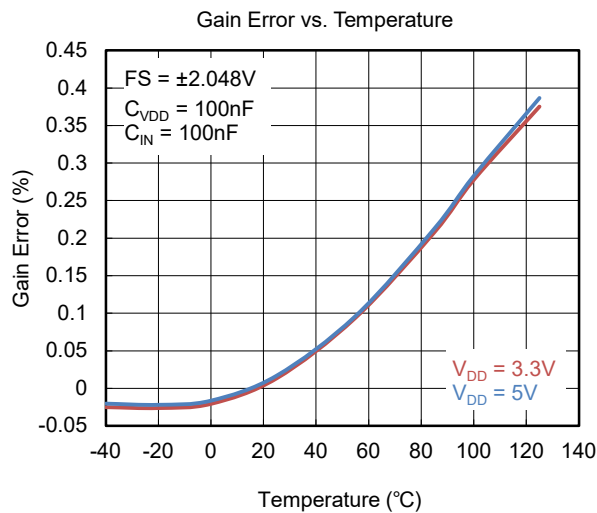
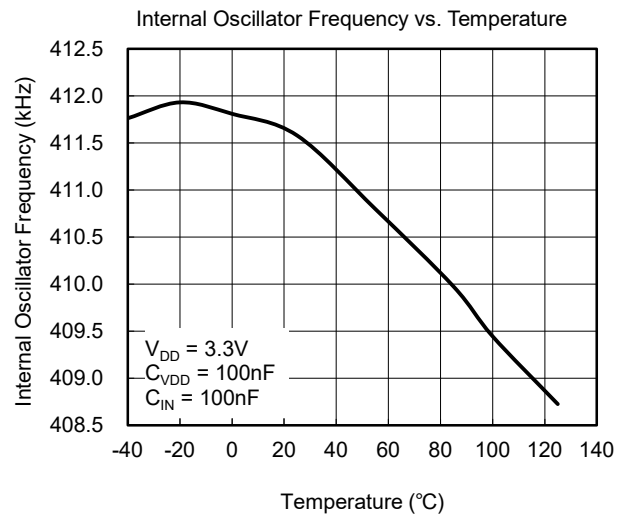
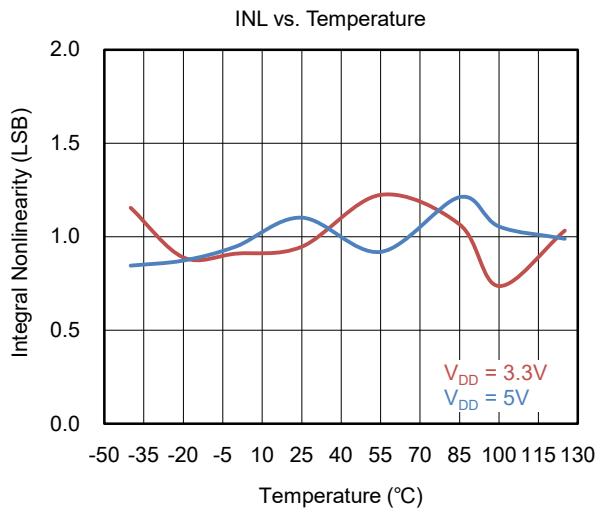


Differential Offset Error vs. Temperature



## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

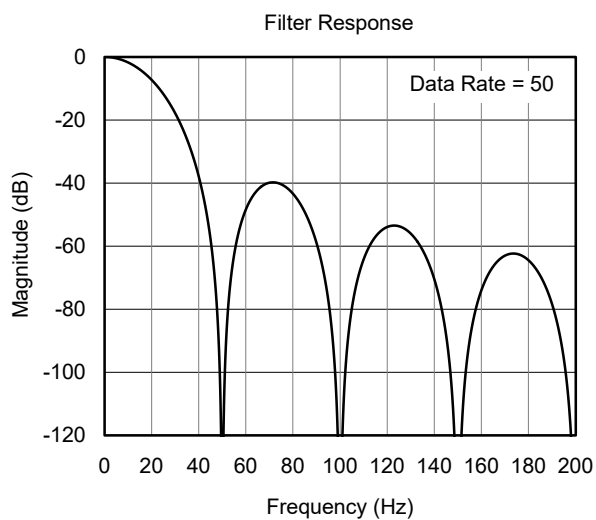
$T_A = +25^\circ\text{C}$ ,  $V_{DD} = 3.3\text{V}$ , Data Rate = 200SPS and Full-Scale (FS) =  $\pm 2.048\text{V}$ , unless otherwise noted.





**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

$T_A = +25^\circ\text{C}$ ,  $V_{DD} = 3.3\text{V}$ , Data Rate = 200SPS and Full-Scale (FS) =  $\pm 2.048\text{V}$ , unless otherwise noted.



## FUNCTIONAL BLOCK DIAGRAM

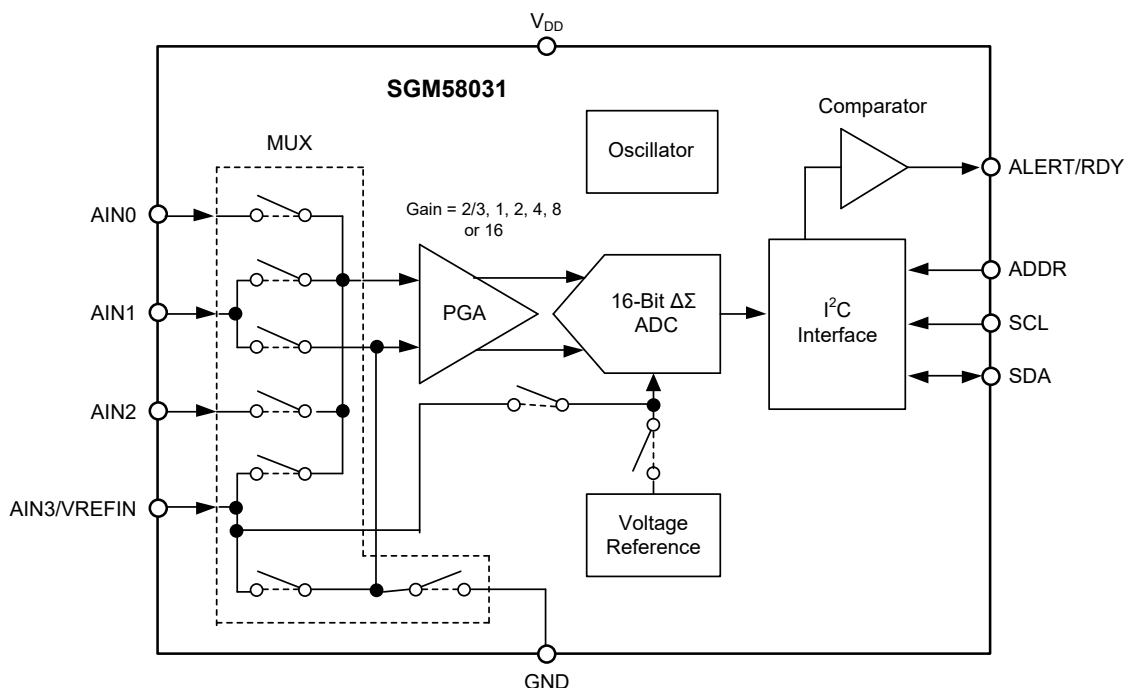


Figure 2. Functional Block Diagram

## DETAILED DESCRIPTION

## Overview

The SGM58031 is a very small, low-power, 16-bit, delta-sigma ( $\Delta\Sigma$ ) analog-to-digital converter (ADC). The SGM58031 is extremely easy to configure and design into a wide variety of applications, and allows precision measurements to be obtained with very little effort. Both experienced and novice users of data converters find designing with the SGM58031 to be intuitive and problem-free.

The SGM58031 consists of a  $\Delta\Sigma$  analog-to-digital (A/D) core with adjustable gain, an internal voltage reference, a clock oscillator, and an I<sup>2</sup>C interface. A feature available on the SGM58031 is a programmable digital comparator that provides an alert on a dedicated pin. All of these features are intended to reduce required external circuitry and improve performance. Figure 2 shows the SGM58031 Functional Block Diagram.

The SGM58031 A/D core measures a differential signal,  $V_{IN}$ , that is the difference of  $A_{INP}$  and  $A_{INN}$ . A MUX is available on the SGM58031. This architecture results in a very strong suppression of any common-mode signals. The converter core consists of a differential,

switched-capacitor  $\Delta\Sigma$  modulator followed by a digital filter. Input signals are compared to the internal voltage reference. The digital filter receives a high-speed bit stream from the modulator and outputs a code proportional to the input voltage.

The SGM58031 has two available conversion modes: single-shot mode and continuous conversion mode. In single-shot mode, the ADC performs one conversion of the input signal upon request and stores the value to an internal result register. The device then enters a low-power shutdown mode. This mode is intended to provide significant power savings in systems that only require periodic conversions or when there are long idle periods between conversions. In continuous conversion mode, the ADC automatically begins a conversion of the input signal as soon as the previous conversion is completed. The rate of continuous conversion is equal to the programmed data rate. Data can be read at any time and always reflect the most recent completed conversion. User can power down the part in continuous conversion mode by setting PD bit to '1' of Config1 register.

## DETAILED DESCRIPTION (continued)

## Quickstart Guide

This section provides a brief example of SGM58031 communications. Refer to subsequent sections of this data sheet for more detailed explanations. Hardware for this design includes: one SGM58031 configured with an I<sup>2</sup>C address of 1001000; a microcontroller with an I<sup>2</sup>C interface; discrete components such as resistors, capacitors, and serial connectors; and a 3V to 5V power supply. Figure 3 shows the basic hardware configuration.

The SGM58031 communicates with the master (microcontroller) through an I<sup>2</sup>C interface. The master provides a clock signal on the SCL pin and data are transferred via the SDA pin. The SGM58031 never drives the SCL pin. For information on programming and debugging the microcontroller being used, refer to the device-specific product data sheet.

The first byte sent by the master should be the SGM58031 address followed by a bit that instructs the SGM58031 to listen for a subsequent byte. The second byte is the Pointer register. Refer to Table 10 and Table 11. The third and fourth bytes sent from the master are written to the register indicated in the second byte.

Refer to Figure 4 and Figure 5 for read and write operation timing diagrams, respectively. All read and write transactions with the SGM58031 must be

preceded by a start condition and followed by a stop condition.

For example, to write to the configuration register to set the SGM58031 to continuous conversion mode and then read the conversion result, send the following bytes in this order:

**Write to Config Register:**

First byte: 0b10010000 (first 7-bit I<sup>2</sup>C address followed by a low read/write bit)

Second byte: 0b00000001 (points to Config register)

Third byte: 0b10000100 (MSB of the Config register to be written)

Fourth byte: 0b10000011 (LSB of the Config register to be written)

**Write to Pointer Register:**

First byte: 0b10010000 (first 7-bit I<sup>2</sup>C address followed by a low read/write bit)

Second byte: 0b00000000 (points to Conversion register)

**Read Conversion Register:**

First byte: 0b10010001 (first 7-bit I<sup>2</sup>C address followed by a high read/write bit)

Second byte: the SGM58031 response with the MSB of the Conversion register

Third byte: the SGM58031 response with the LSB of the Conversion register

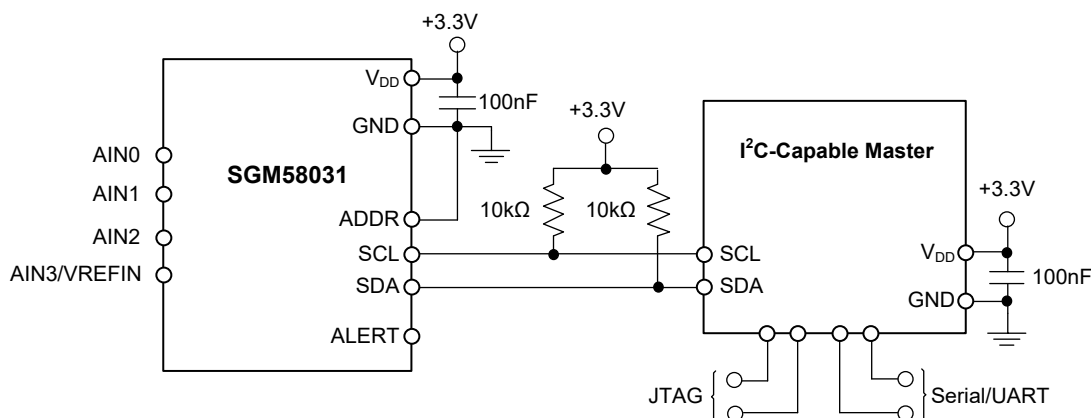
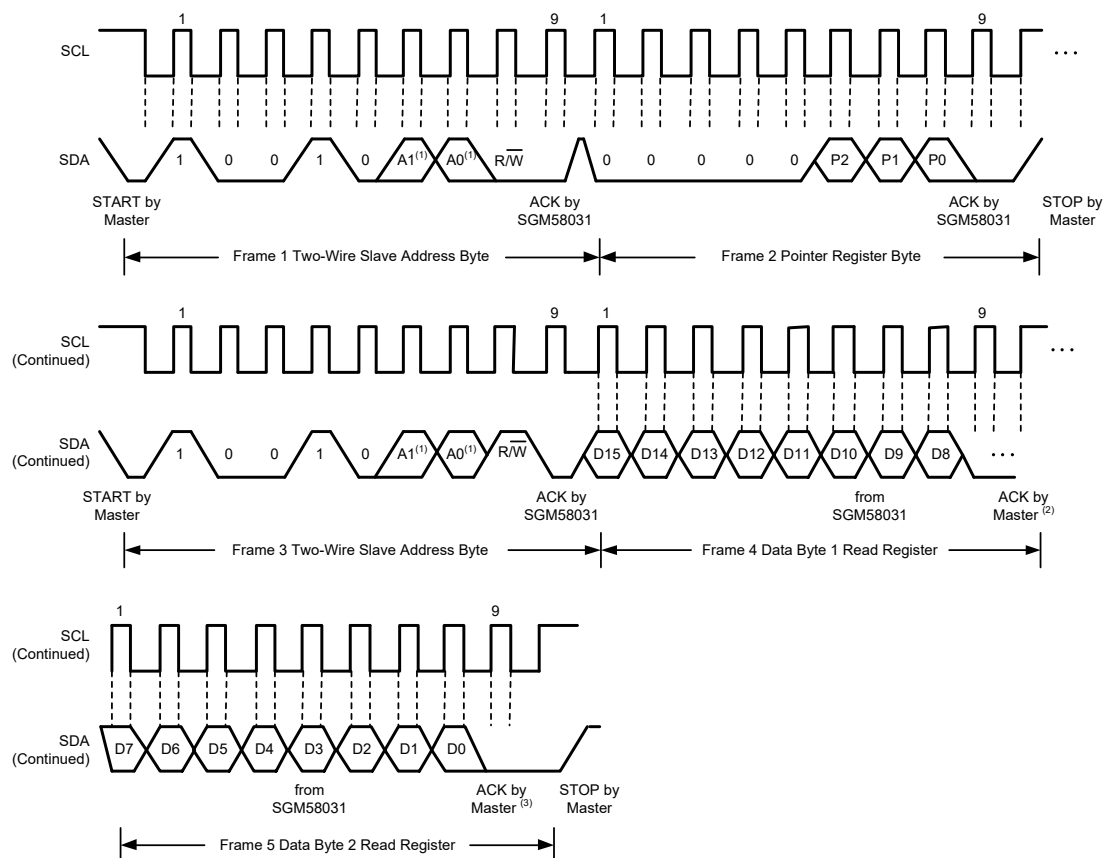


Figure 3. Basic Hardware Configuration

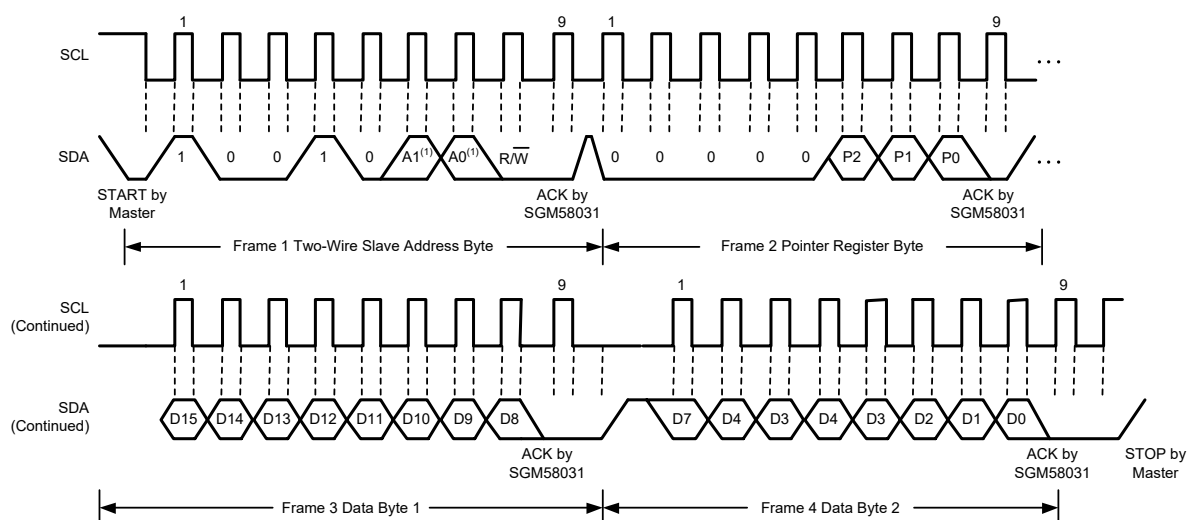
## DETAILED DESCRIPTION (continued)



### NOTES:

1. The values of A0 and A1 are determined by the ADDR pin.
2. Master can leave SDA high to terminate a single-byte read operation.
3. Master can leave SDA high to terminate a two-byte read operation.

**Figure 4. Two-Wire Timing Diagram for Reading Word Register**



NOTE: 1. The values of A0 and A1 are determined by the ADDR pin.

**Figure 5. Two-Wire Timing Diagram for Write Word Format**

## DETAILED DESCRIPTION (continued)

## Multiplexer

The SGM58031 contains an input multiplexer, as shown in Figure 6. Either four single-ended or two differential signals can be measured. Additionally, AIN0 to AIN2 may be measured differentially to AIN3. The multiplexer is configured by MUX[2:0] bits in the Config register. When single-ended signals are measured, the negative input of the ADC is internally connected to GND by a switch within the multiplexer.

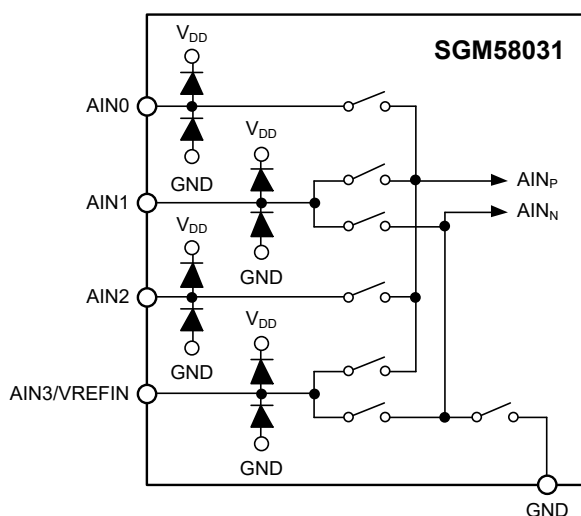


Figure 6. SGM58031 MUX

When measuring single-ended inputs it is important to note that the negative range of the output codes are not used. These codes are for measuring negative differential signals such as  $(A_{INP} - A_{INN}) < 0$ . ESD diodes to  $V_{DD}$  and GND protect the inputs on the device. To prevent the ESD diodes from turning on, the absolute voltage on any input must stay within the following range:

$$GND - 0.3V < AINx < V_{DD} + 0.3V$$

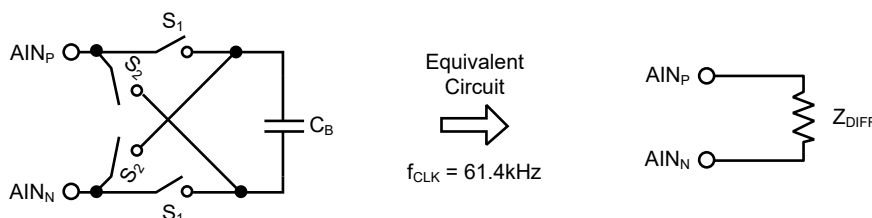


Figure 7. Simplified Analog Input Circuit

If it is possible that the voltages on the input pins may violate these conditions, external Schottky clamp diodes and/or series resistors may be required to limit the input current to safe values (see the Absolute Maximum Ratings).

Also, overdriving one unused input on the SGM58031 may affect conversions taking place on other input pins. If overdrive on unused inputs is possible, again it is recommended to clamp the signal with external Schottky diodes.

## Analog Inputs

The SGM58031 uses a switched-capacitor input stage where capacitors are continuously charged and then discharged to measure the voltage between  $A_{INP}$  and  $A_{INN}$ . The capacitors used are small, and to external circuitry the average loading appears resistive. The resistance is set by the capacitor values and the rate at which they are switched. This charging draws a very small transient current from the source driving the SGM58031 analog inputs. The average value of this current can be used to calculate the effective impedance ( $R_{EFF}$ ) where  $R_{EFF} = V_{IN}/I_{AVERAGE}$ .

The differential input impedance is measured by applying a differential signal to  $A_{INP}$  and  $A_{INN}$  inputs. The differential current scales with the PGA gain setting. In Figure 7, the differential input impedance is  $Z_{DIFF}$ . Table 2 describes the typical differential input impedance.

## DETAILED DESCRIPTION (continued)

The typical value of the input impedance cannot be neglected. Unless the input source has a low impedance, the SGM58031 input impedance may affect the measurement accuracy. For sources with high output impedance, buffering may be necessary. Active buffers introduce noise, and also introduce offset and gain errors. All of these factors should be considered in high-accuracy applications.

Because the clock oscillator frequency drifts slightly with temperature, the input impedances also drift. For many applications, this input impedance drift can be ignored, and the values given in Table 2 for typical input impedance are valid.

Table 2. Differential Input Impedance

FS (V)	Differential Input Impedance
$\pm 6.144\text{V}^{(1)}$	37.5M $\Omega$
$\pm 4.096\text{V}^{(1)}$	25M $\Omega$
$\pm 2.048\text{V}$	12.5M $\Omega$
$\pm 1.024\text{V}$	6.25M $\Omega$
$\pm 0.512\text{V}$	6.25M $\Omega$
$\pm 0.256\text{V}$	6.25M $\Omega$

NOTE: 1. This parameter expresses the full-scale range of the ADC scaling. In no event should more than  $V_{DD} + 0.3\text{V}$  be applied to this device.

## Full-Scale Input

A programmable gain amplifier (PGA) is implemented before the  $\Delta\Sigma$  core of the SGM58031. The PGA can be set to gains of 2/3, 1, 2, 4, 8 or 16. Table 3 and Table 4 show the corresponding full-scale (FS) ranges.

The PGA is configured by PGA[2:0] bits in the Config register. The PGA = 2/3 setting allows input measurement to extend up to the supply voltage when  $V_{DD}$  is larger than 4V. Note though that in this case (as well as for PGA = 1 and  $V_{DD} < 4\text{V}$ ), it is not possible to reach a full-scale output code on the ADC. Analog input voltages may never exceed the analog input voltage limits.

Table 3. PGA Gain Full-Scale Range with Internal Reference

PGA Setting	FS (V)
2/3	$\pm 6.144\text{V}^{(1)}$
1	$\pm 4.096\text{V}^{(1)}$
2	$\pm 2.048\text{V}$
4	$\pm 1.024\text{V}$
8	$\pm 0.512\text{V}$
16	$\pm 0.256\text{V}$

NOTE: 1. This parameter expresses the full-scale range of the ADC scaling. In no event should more than  $V_{DD} + 0.3\text{V}$  be applied to this device.

Table 4. PGA Gain Full-Scale Range with External Reference

PGA Setting	FS (V)
2/3	$\pm 3 \times V_{REF}$
1	$\pm 2 \times V_{REF}$
2	$\pm V_{REF}$
4	$\pm V_{REF}/2$
8	$\pm V_{REF}/4$
16	$\pm V_{REF}/8$

## Data Format

The SGM58031 provides 16 bits of data in binary two's complement format. The positive full-scale input produces an output code of 7FFFh and the negative full-scale input produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale. Table 5 summarizes the ideal output codes for different input signals. Figure 8 shows code transitions versus input voltage.

Table 5. Input Signal versus Ideal Output Code

Input Signal, $V_{IN}$ ( $A_{INP} - A_{INN}$ )	Ideal Output Code <sup>(1)</sup>
$\geq FS (2^{15} - 1)/2^{15}$	7FFFh
$+FS/2^{15}$	0001h
0	0
$-FS/2^{15}$	FFFFh
$\leq -FS$	8000h

NOTE: 1. Excludes the effects of noise, INL, offset, and gain errors.

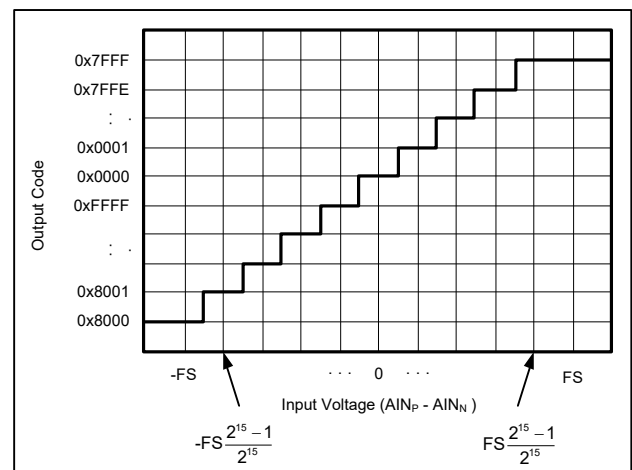


Figure 8. SGM58031 Code Transition Diagram

**DETAILED DESCRIPTION (continued)****Aliasing**

As with any data converter, if the input signal contains frequencies greater than half the data rate, aliasing occurs. To prevent aliasing, the input signal must be band limited. Some signals are inherently bandlimited. For example, the output of a thermocouple, which has a limited rate of change. Nevertheless, they can contain noise and interference components. These components can fold back into the sampling band in the same way as with any other signal.

The SGM58031 digital filter provides some attenuation of high-frequency noise, but the digital Sinc filter frequency response cannot completely replace an anti-aliasing filter. For a few applications, some external filtering may be needed; in such instances, a simple RC filter is adequate.

When designing an input filter circuit, be sure to take into account the interaction between the filter network and the input impedance of the SGM58031.

**Operating Modes**

The SGM58031 operates in one of two modes: continuous conversion mode or single-shot mode. In continuous conversion mode, the SGM58031 continuously performs conversions. Once a conversion has been completed, the SGM58031 places the result in the Conversion register and immediately begins another conversion. In single-shot mode, the SGM58031 waits until the OS bit is set high. Once asserted, the bit is set to '0', indicating that a conversion is currently in progress. Once conversion data are ready, the OS bit reasserts and the device powers down. Writing a '1' to the OS bit during a conversion has no effect.

**Power-Up and Reset**

When the SGM58031 powers up, a reset is performed. As part of the reset process, the SGM58031 sets all of the bits in the Config register to the respective default settings.

The SGM58031 responds to the I<sup>2</sup>C general call reset command. When the SGM58031 receives a general call reset, an internal reset is performed as if the device had been powered on.

**Duty Cycling for Low Power**

For many applications, the improved performance at low data rates may not be required. For these applications, the SGM58031 supports duty cycling that can yield significant power savings by periodically requesting high data rate readings at an effectively lower data rate. For example, an SGM58031 in power-down mode with a data rate set to 960SPS could be operated by a microcontroller that instructs a single-shot conversion every 125ms (8SPS). Because a conversion at 960SPS only requires about 3.2ms, the SGM58031 enters power-down mode for the remaining 121.8ms. In this configuration, the SGM58031 consumes about 1/40<sup>th</sup> the power of the SGM58031 operated in continuous conversion mode. The rate of duty cycling is completely arbitrary and is defined by the master controller. The SGM58031 offers lower data rates that do not implement duty cycling and offer improved noise performance if it is needed.

**Data Rate****Table 6. ADC Output Data Rate (SPS)**

DR[2:0] Bits in Config Register	DR_SEL Bit in Config1 Register	
	DR_SEL = 0	SR_SEL = 1
000	6.25Hz	7.5Hz
001	12.5Hz	15Hz
010	25Hz	30Hz
011	50Hz	60Hz
100	100Hz	120Hz
101	200Hz	240Hz
110	400Hz	480Hz
111	800Hz	960HZ

## DETAILED DESCRIPTION (continued)

## Comparator

The SGM58031 is each equipped with a comparator that can issue an alert on the ALERT/RDY pin. This feature can significantly reduce external circuitry in many applications. The comparator can be implemented as either a traditional comparator or a window comparator via the COMP\_MODE bit in the Config register. When implemented as a traditional comparator, the ALERT/RDY pin asserts (active low by default) when conversion data exceed the limit set in the high threshold register. The comparator then deasserts when the input signal falls below the low threshold register value. In window comparator mode, the ALERT/RDY pin asserts if conversion data exceed the high threshold register or fall below the low threshold register.

In either window or traditional comparator mode, the comparator can be configured to latch once asserted

by the COMP\_LAT bit in the Config register. This setting causes the assertion to remain even if the input signal is not beyond the bounds of the threshold registers. This latched assertion can be cleared by issuing an SMBus alert response or by reading the Conversion register. The COMP\_POL bit in the Config register configures the ALERT/RDY pin as active high or active low. Operational diagrams for the comparator modes are shown in Figure 9 and Figure 10.

The comparator can be configured to activate the ALERT/RDY pin after a set number of successive readings exceed the threshold. The comparator can be configured to wait for one, two, or four readings beyond the threshold before activating the ALERT/RDY pin by changing the COMP\_QUE[1:0] bits in the Config register. The COMP\_QUE[1:0] bits can also disable the comparator function.

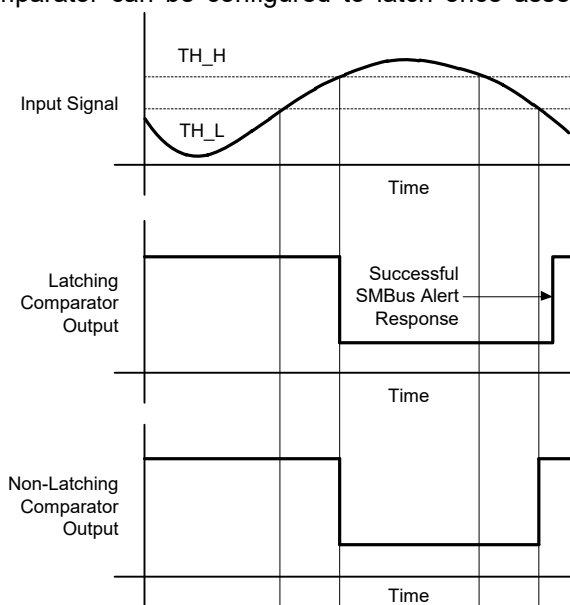


Figure 9. Alert Pin Timing Diagram when Configured as a Traditional Comparator

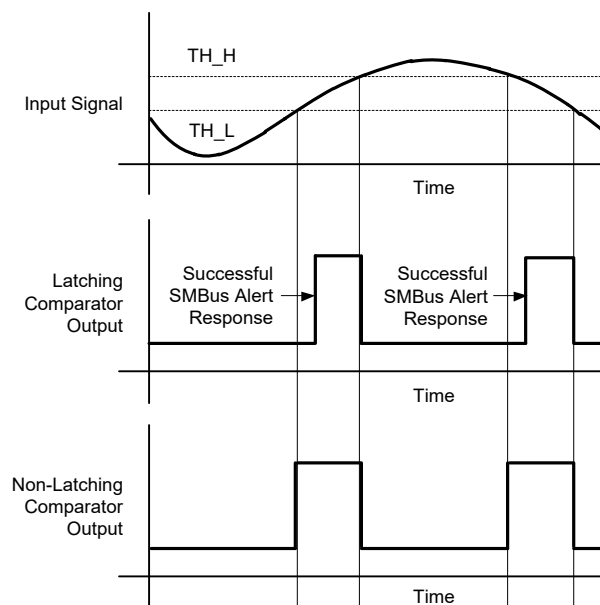


Figure 10. Alert Pin Timing Diagram when Configured as a Window Comparator

## ADC Noise

Table 7. ADC Noise with Internal Reference (RMS in  $\mu\text{V}$ )

DR FS	800	400	200	100	50	25	12.5	6.25
6.144	187.5	187.5	187.5	187.5	187.5	187.5	187.5	187.5
4.096	125	125	125	125	125	125	125	125
2.048	62.5	62.5	62.5	62.5	62.5	62.5	62.5	62.5
1.024	31.25	31.25	31.25	31.25	31.25	31.25	31.25	31.25
0.512	15.62	15.62	15.62	15.62	15.62	15.62	15.62	15.62
0.256	7.81	7.81	7.81	7.81	7.81	7.81	7.81	7.81



**DETAILED DESCRIPTION (continued)**Table 8. ADC ENOB (ENOB =  $(20\log (FS/Noise\_RMS) - 1.76)/6.02$ )

DR FS	800	400	200	100	50	25	12.5	6.25
6.144	16	16	16	16	16	16	16	16
4.096	16	16	16	16	16	16	16	16
2.048	16	16	16	16	16	16	16	16
1.024	16	16	16	16	16	16	16	16
0.512	16	16	16	16	16	16	16	16
0.256	16	16	16	16	16	16	16	16

**Conversion Ready Pin**

The ALERT/RDY pin can also be configured as a conversion ready pin. This mode of operation can be realized if the MSB of the high threshold register is set to '1' and the MSB of the low threshold register is set to '0'. The COMP\_POL bit continues to function and the COMP\_QUE[1:0] bits can disable the pin; however, the COMP\_MODE and COMP\_LAT bits no longer control any function. When configured as a conversion ready pin, ALERT/RDY pin requires a pull-up resistor. When in continuous conversion mode, the SGM58031 provides a brief (8μs) pulse on the ALERT/RDY pin at the end of each conversion. When in single-shot shutdown mode, the ALERT/RDY pin asserts low at the end of a conversion if the COMP\_POL bit is set to '0', and clears ALERT/RDY pin by next conversion.

**Digital Filter**

The devices offer digital filter for filtering the digital data stream coming from the delta-sigma modulator. The implementation of the digital filter is determined by the ADC data rate setting. When data rate is configured as 120, 100, 60, 50, 30, 25, 15, 12.5, 7.5 and 6.25, the device uses a third-order Sinc filter (Sinc3). When data rate is configured as 200, 240, 400, 480, 800 and 960, the device uses a fourth-order Sinc filter (Sinc4).

When ALERT/RDY is used as the conversion completed indication pin, its default logic state is high (pulled up by the external resistor) during the conversion. When the device works in continuous mode, the ALERT/RDY pin will go low and remain low

for about 8μs, generating an 8μs logic low pulse at the end of each conversion cycle. When the device works in single-shot mode and the Sinc3 filter is used, the ALERT/RDY pin will go logic low after the third data conversion is finished and remain low until the device begins the next new conversion (OS bit is set to '1' again), and the ALERT/RDY pin goes logic high again during the new conversion. When the device works in single-shot mode and the Sinc4 filter is used, the ALERT/RDY pin will go low after the fourth data conversion is finished and remain low until the device begins the next new conversion (OS bit is set to '1' again), and the ALERT/RDY pin goes logic high again during the new conversion.

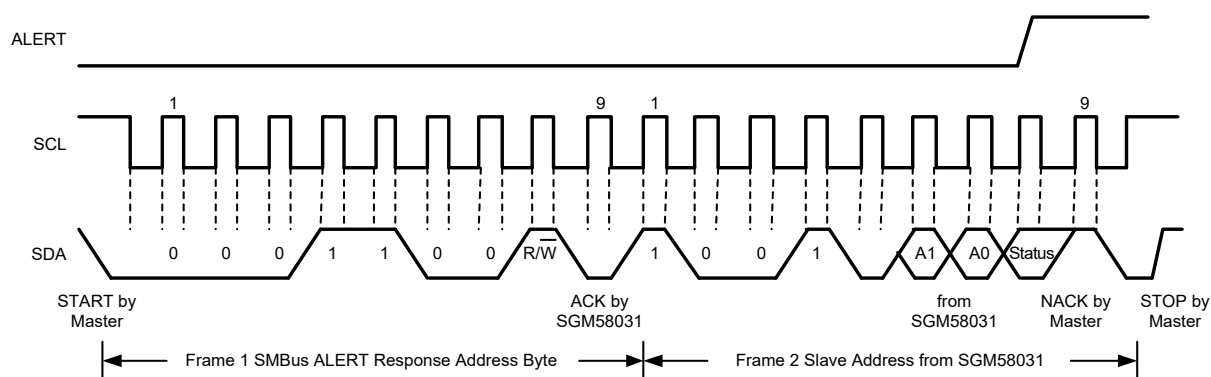
**SMBus Alert Response**

When configured in latching mode (COMP\_LAT = '1' in the Config register), the ALERT/RDY pin can be implemented with an SMBus alert. The pin asserts if the comparator detects a conversion that exceeds an upper or lower threshold. This interrupt is latched and can be cleared only by reading conversion data, or by issuing a successful SMBus alert response and reading the asserting device I<sup>2</sup>C address. If conversion data exceed the upper or lower thresholds after being cleared, the pin reasserts. This assertion does not affect conversions that are already in progress. The ALERT/RDY pin, as with the SDA pin, is an open-drain pin. This architecture allows several devices to share the same interface bus. When disabled, the pin holds a high state so that it does not interfere with other devices on the same bus line.

## DETAILED DESCRIPTION (continued)

When the master senses that the ALERT/RDY pin has latched, it issues an SMBus alert command (00011001) to the I<sup>2</sup>C bus. Any SGM58031 data converters on the I<sup>2</sup>C bus with the ALERT/RDY pins asserted respond to the command with the slave address. In the event that two or more SGM58031 data converters present on the bus assert the latched ALERT/RDY pin, arbitration during the address response portion of the SMBus alert decides which device clears its assertion. The device

with the lowest I<sup>2</sup>C address always wins arbitration. If a device loses arbitration, it does not clear the comparator output pin assertion. The master then repeats the SMBus alert response until all devices have had the respective assertions cleared. In window comparator mode, the SMBus alert status bit indicates a '1' if signals exceed the high threshold and a '0' if signals exceed the low threshold. Timing Diagram for SMBus Alert Response is shown in Figure 11.



NOTE: 1. The values of A0 and A1 are determined by the ADDR pin.

Figure 11. Timing Diagram for SMBus ALERT Response

I<sup>2</sup>C Interface

The SGM58031 communicates through an I<sup>2</sup>C interface. I<sup>2</sup>C is a two-wire open-drain interface that supports multiple devices and masters on a single bus. Devices on the I<sup>2</sup>C bus only drive the bus lines low by connecting them to ground; they never drive the bus lines high. Instead, the bus wires are pulled high by pull-up resistors, so the bus wires are high when no device is driving them low. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

Communication on the I<sup>2</sup>C bus always takes place between two devices, one acting as the master and the other as the slave. Both masters and slaves can read and write, but slaves can only do so under the direction of the master. Some I<sup>2</sup>C devices can act as masters or slaves, but the SGM58031 can only act as slave devices.

An I<sup>2</sup>C bus consists of two lines, SDA and SCL. SDA carries data; SCL provides the clock. All data are transmitted across the I<sup>2</sup>C bus in groups of 8 bits. To send a bit on the I<sup>2</sup>C bus, the SDA line is driven to the appropriate level while SCL is low (a low on SDA indicates the bit is '0'; a high indicates the bit is '1').

Once the SDA line settles, the SCL line is brought high, then low. This pulse on SCL clocks the SDA bit into the receiver shift register. If the I<sup>2</sup>C bus is held idle (SCL = low) for more than 25ms, the bus times out.

The I<sup>2</sup>C bus is bidirectional: the SDA line is used for both transmitting and receiving data. When the master reads from a slave, the slave drives the data line; when the master sends to a slave, the master drives the data line. The master always drives the clock line. The SGM58031 never drives SCL, because they cannot act as a master. On the SGM58031, SCL is an input only.

Most of the time the bus is idle; no communication occurs, and both lines are high. When communication is taking place, the bus is active. Only master devices can start a communication and initiate a START condition on the bus. Normally, the data line is only allowed to change state while the clock line is low. If the data line changes state while the clock line is high, it is either a START condition or a STOP condition. A START condition occurs when the clock line is high and the data line goes from high to low. A STOP condition occurs when the clock line is high and the data line goes from low to high.

**DETAILED DESCRIPTION (continued)**

After the master issues a START condition, it sends a byte that indicates which slave device it wants to communicate with. This byte is called the address byte. Each device on an I<sup>2</sup>C bus has a unique 7-bit address to which it responds. The master sends an address in the address byte, together with a bit that indicates whether it wishes to read from or write to the slave device.

Every byte transmitted on the I<sup>2</sup>C bus, whether it is address or data, is acknowledged with an acknowledge bit. When the master has finished sending a byte (eight data bits) to a slave, it stops driving SDA and waits for the slave to acknowledge the byte. The slave acknowledges the byte by pulling SDA low. The master then sends a clock pulse to clock the acknowledge bit. Similarly, when the master has finished reading a byte, it pulls SDA low to acknowledge this to the slave. It then sends a clock pulse to clock the bit. (The master always drives the clock line.)

A not-acknowledge is performed by simply leaving SDA high during an acknowledge cycle. If a device is not present on the bus, and the master attempts to address it, it receives a not-acknowledge because no device is present at that address to pull the line low.

When the master has finished communicating with a slave, it may issue a STOP condition. When a STOP condition is issued, the bus becomes idle again. The master may also issue another START condition. When a START condition is issued while the bus is active, it is called a repeated START condition. See the Timing Requirements section for a timing diagram showing the SGM58031 I<sup>2</sup>C transaction.

**I<sup>2</sup>C Address Selection**

The SGM58031 has one address pin, ADDR, that sets the I<sup>2</sup>C address. This pin can be connected to ground, V<sub>DD</sub>, SDA, or SCL, allowing four addresses to be selected with one pin as shown in Table 9. The state of the address pin ADDR is sampled continuously.

**Table 9. ADDR Pin Connection and Corresponding Slave Address**

ADDR Pin	Slave Address
Ground	1001000
V <sub>DD</sub>	1001001
SDA	1001010
SCL	1001011

**I<sup>2</sup>C General Call**

The SGM58031 responds to the I<sup>2</sup>C general call address (0000000) if the eighth bit is '0'. The device acknowledges the general call address and responds to commands in the second byte. If the second byte is 00000110 (06h), the SGM58031 resets the internal registers and enters power-down mode.

**I<sup>2</sup>C Speed Modes**

The I<sup>2</sup>C bus operates at one of three speeds. Standard mode allows a clock frequency of up to 100kHz; fast mode permits a clock frequency of up to 400kHz; and high-speed mode (also called HS mode) allows a clock frequency of up to 3.4MHz. The SGM58031 is fully compatible with all three modes. (See note in Electrical Spec for details.)

No special action is required to use the SGM58031 in standard or fast mode, but HS mode must be activated. To activate HS mode, send a special address byte of 00001XXX following the START condition, where XXX are bits unique to the HS-capable master. This byte is called the HS master code. (Note that this is different from normal address bytes; the eighth bit does not indicate read/write status.) The SGM58031 does not acknowledge this byte; the I<sup>2</sup>C specification prohibits acknowledgment of the HS master code. Upon receiving a master code, the SGM58031 switch on HS mode filters, and communicates at up to 3.4MHz. The SGM58031 switches out of HS mode with the next STOP condition. For more information on HS mode, consult the I<sup>2</sup>C specification.

**Slave Mode Operations**

The SGM58031 can act as either slave receiver or slave transmitter. As a slave device, the SGM58031 cannot drive the SCL line.

**Receive Mode:**

In slave receive mode the first byte transmitted from the master to the slave is the address with the R/ $\bar{W}$  bit low. This byte allows the slave to be written to. The next byte transmitted by the master is the Pointer register byte. The SGM58031 then acknowledges receipt of the Pointer register byte. The next two bytes are written to the address given by the Pointer register. The SGM58031 acknowledges each byte sent. Register bytes are sent with the most significant byte first, followed by the least significant byte.

**DETAILED DESCRIPTION (continued)****Transmit Mode:**

In slave transmit mode, the first byte transmitted by the master is the 7-bit slave address followed by the high  $R/\bar{W}$  bit. This byte places the slave into transmit mode and indicates that the SGM58031 is being read from. The next byte transmitted by the slave is the most significant byte of the register that is indicated by the Pointer register. This byte is followed by an acknowledgment from the master. The remaining least significant byte is then sent by the slave and is followed by an acknowledgment from the master. The master may terminate transmission after any byte by not acknowledging or issuing a START or STOP condition.

**Writing/Reading the Registers**

To access a specific register from the SGM58031, the master must first write an appropriate value to the Pointer register. The Pointer register is written directly after the slave address byte, low  $R/\bar{W}$  bit, and a successful slave acknowledgment. After the Pointer register is written, the slave acknowledges and the master issues a STOP or a repeated START condition.

When reading from the SGM58031, the previous value written to the Pointer register determines the register that is read from. To change which register is read, a new value must be written to the Pointer register. To write a new value to the Pointer register, the master issues a slave address byte with the  $R/\bar{W}$  bit low, followed by the Pointer register byte. No additional data need to be transmitted, and a STOP condition can be issued by the master. The master may now issue a

START condition and send the slave address byte with the  $R/\bar{W}$  bit high to begin the read. Table 14 details this sequence. If repeated reads from the same register are desired, there is no need to continually send Pointer register bytes, because the SGM58031 stores the value of the Pointer register until it is modified by a write operation. However, every write operation requires the Pointer register to be written.

**Register Address**

The SGM58031 has seven registers that are accessible via the I<sup>2</sup>C port. The Conversion register contains the result of the last conversion. The Config register allows the user to change the SGM58031 operating modes and query the status of the devices. Two registers, Lo\_Thresh and Hi\_Thresh, set the threshold values used for the comparator function. The seven registers are accessed by writing to the Pointer register byte; see Figure 4. Table 10 and Table 11 indicate the Pointer register byte map.

**Table 10. User Register Address**

Address	Register
0x0	Conversion Register
0x1	Config Register
0x2	Lo_Thresh
0x3	Hi_Thresh
0x4	Config1 Register
0x5	Chip ID
0x6	GN_Trim1 for EXT_REF

**Pointer Register****Table 11. Pointer Register Byte (Write-Only)**

7	6	5	4	3	2	1	0
0	0	0	0	0	Register Address		

**Conversion Register**

The 16-bit register contains the result of the last conversion in binary two's complement format. Following reset or power-up, the Conversion register is cleared to '0', and remains '0' until the first conversion is completed. The register format is shown in Table 12.

**Table 12. Conversion Register 16-Bit Mode (Read-Only)**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: Default Value = 0000h.

## DETAILED DESCRIPTION (continued)

### Config Register

The 16-bit register can be used to control the SGM58031 operating mode, input selection, data rate, PGA settings, and comparator modes. The register format is shown in Table 13.

**Table 13. Config Register (Read/Write)**

Bit	15	14	13	12	11	10	9	8
Name	OS	MUX[2:0]			PGA[2:0]			MODE
Bit	7	6	5	4	3	2	1	0
Name	DR[2:0]			COMP_MODE	COMP_POL	COMP_LAT	COMP_QUE[1:0]	

NOTE: Default Value = 8583h.

#### Bit [15] OS: Operational Status/Single-Shot Conversion Start

This bit determines the operational status of the device.

This bit can only be written when in power-down mode.

For a write status:

0: No effect

1: Begin a single conversion (when in power-down mode)

For a read status:

0: Device is currently performing a conversion

1: Device is not currently performing a conversion

#### Bits [14:12] MUX[2:0]: Input Multiplexer Configuration (default = 000)

These bits configure the input multiplexer.

000:  $A_{IN_P} = A_{IN0}$  and  $A_{IN_N} = A_{IN1}$  (default)

001:  $A_{IN_P} = A_{IN0}$  and  $A_{IN_N} = A_{IN3}$

010:  $A_{IN_P} = A_{IN1}$  and  $A_{IN_N} = A_{IN3}$

011:  $A_{IN_P} = A_{IN2}$  and  $A_{IN_N} = A_{IN3}$

100:  $A_{IN_P} = A_{IN0}$  and  $A_{IN_N} = GND$

101:  $A_{IN_P} = A_{IN1}$  and  $A_{IN_N} = GND$

110:  $A_{IN_P} = A_{IN2}$  and  $A_{IN_N} = GND$

111:  $A_{IN_P} = A_{IN3}$  and  $A_{IN_N} = GND$

#### Bits [11:9] PGA[2:0]: Programmable Gain Amplifier Configuration (default = 010)

These bits configure the programmable gain amplifier.

000:  $FS = \pm 6.144V$  <sup>(1)</sup>

001:  $FS = \pm 4.096V$  <sup>(1)</sup>

010:  $FS = \pm 2.048V$  (default)

011:  $FS = \pm 1.024V$

100:  $FS = \pm 0.512V$

101:  $FS = \pm 0.256V$

110:  $FS = \pm 0.256V$

111:  $FS = \pm 0.256V$

#### Bit [8] MODE: Device Operating Mode (default = 1)

This bit controls the current operational mode of the SGM58031.

0: Continuous conversion mode

1: Power-down single-shot mode (default)

**DETAILED DESCRIPTION (continued)****Bits [7:5] DR[2:0]: DATA RATE (default = 100)**

These bits control the data rate setting. See Table 6.

**Bit [4] COMP\_MODE: Comparator mode (default = 0)**

This bit controls the comparator mode of operation. It changes whether the comparator is implemented as a traditional comparator (COMP\_MODE = '0') or as a window comparator (COMP\_MODE = '1').

0: Traditional comparator with hysteresis (default)

1: Window comparator

**Bit [3] COMP\_POL: Comparator polarity (default = 0)**

This bit controls the polarity of the ALERT/RDY pin. When COMP\_POL = '0' the comparator output is active low. When COMP\_POL = '1' the ALERT/RDY pin is active high.

0: Active low (default)

1: Active high

**Bit [2] COMP\_LAT: Latching comparator (default = 0)**

This bit controls whether the ALERT/RDY pin latches once asserted or clears once conversions are within the margin of the upper and lower threshold values. When COMP\_LAT = '0', the ALERT/RDY pin does not latch when asserted. When COMP\_LAT = '1', the asserted ALERT/RDY pin remains latched until conversion data are read by the master or an appropriate SMBus alert response is sent by the master, the device responds with its address, and it is the lowest address currently asserting the ALERT/RDY bus line.

0: Non-latching comparator (default)

1: Latching comparator

**Bits [1:0] COMP\_QUE[1:0]: Comparator queue and disable (default = 11)**

These bits perform two functions. When set to '11', they disable the comparator function and put the ALERT/RDY pin into a high state. When set to any other value, they control the number of successive conversions exceeding the upper or lower thresholds required before asserting the ALERT/RDY pin.

00: Assert after one conversion

01: Assert after two conversions

10: Assert after four conversions

11: Disable comparator (default)

NOTE: This parameter expresses the full-scale range of the ADC scaling. In no event should more than  $V_{DD} + 0.3V$  be applied to this device.

**DETAILED DESCRIPTION (continued)****Lo\_Thresh and Hi\_Thresh Registers**

The upper and lower threshold values used by the comparator are stored in two 16-bit registers. These registers store values in the same format that the output register displays values; that is, they are stored in two's complement format. Because it is implemented as a digital comparator, special attention should be taken to readjust values whenever PGA settings are changed.

A secondary conversion ready function of the comparator output pin can be realized by setting the Hi\_Thresh register MSB to '1' and the Lo\_Thresh register MSB to '0'. However, in all other cases, the Hi\_Thresh register must be larger than the Lo\_Thresh register. The threshold register formats are shown in Table 14. When set to RDY mode, the ALERT/RDY pin outputs the OS bit when in single-shot mode and pulses when in continuous conversion mode.

**Table 14. Lo\_Thresh and Hi\_Thresh Registers**

Register	Lo_Thresh (Read/Write)							
Bit	15	14	13	12	11	10	9	8
Name	Lo_Thresh15	Lo_Thresh14	Lo_Thresh13	Lo_Thresh12	Lo_Thresh11	Lo_Thresh10	Lo_Thresh9	Lo_Thresh8
Bit	7	6	5	4	3	2	1	0
Name	Lo_Thresh7	Lo_Thresh6	Lo_Thresh5	Lo_Thresh4	Lo_Thresh3	Lo_Thresh2	Lo_Thresh1	Lo_Thresh0
Register	Hi_Thresh (Read/Write)							
Bit	15	14	13	12	11	10	9	8
Name	Hi_Thresh15	Hi_Thresh14	Hi_Thresh13	Hi_Thresh12	Hi_Thresh11	Hi_Thresh10	Hi_Thresh9	Hi_Thresh8
Bit	7	6	5	4	3	2	1	0
Name	Hi_Thresh7	Hi_Thresh6	Hi_Thresh5	Hi_Thresh4	Hi_Thresh3	Hi_Thresh2	Hi_Thresh1	Hi_Thresh0

NOTE: Lo\_Thresh Default Value = 8000h, Hi\_Thresh Default Value = 7FFFh.

## DETAILED DESCRIPTION (continued)

### Config1 Register

Table 15. 16-Bit Config Register for New Controls

Bit	15	14	13	12	11	10	9	8
Name	N/A	N/A	N/A	N/A	N/A	N/A	N/A	PD
Bit	7	6	5	4	3	2	1	0
Name	DR_SEL	BURNOUT	INT_DIO	BUS_FLEX	EXT_REF	N/A	N/A	N/A

#### PD Bit [8]: (default = 0)

Writing '1' to PD powers down this part, and this PD bit is automatically cleared internally. Another continuous/single conversion can be carried out again without the need to clear this bit.

#### DR\_SEL Bit [7]: (default = 0)

- 0: DR[2:0] = 000~111 for conversion rate of 6.25Hz, 12.5Hz, 25Hz, 50Hz, 100Hz, 200Hz, 400Hz and 800Hz.
- 1: DR[2:0] = 000~111 for conversion rate of 7.5Hz, 15Hz, 30Hz, 60Hz, 120Hz, 240Hz, 480Hz and 960Hz.

#### BURNOUT Bit [6]: (default = 0)

- 0: No current sourced.
- 1: Source a pair of 2μA current to selected pair of AINs.

#### INT\_DIO Bit [5]: (default = 0)

- 0: None. (default)
- 1: Select internal diode as ADC input.

#### BUS\_FLEX Bit [4]: (default = 0)

- 0: Disable leakage blocking circuit for the scenario that I<sup>2</sup>C bus voltage is lower than V<sub>DD</sub> of the part. The I<sup>2</sup>C interface is still functional but V<sub>DD</sub> sees leakage when V<sub>BUS</sub> < V<sub>DD</sub> - 0.3V.
- 1: Bus voltage can be lower than V<sub>DD</sub> without causing leakage. The V<sub>DD</sub> range is 3V to 5.5V and the I<sup>2</sup>C bus voltage should be limited to 3V to 5.5V.

#### EXT\_REF Bit [3]: (default = 0)

- 0: None. (default)
- 1: Use AIN3 as external reference for ADC.



## DETAILED DESCRIPTION (continued)

### Chip\_ID

**Table 16. 16-Bit Read Only Register for Identifying Chip ID and Its Subversions**

Bit	15	14	13	12	11	10	9	8
Description	N/A	N/A	N/A	ID[4:0]				
Default Value	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Description	VER[2:0]			N/A	N/A	N/A	N/A	N/A
Default Value	1	0	0	0	0	0	0	0

### GN\_Trim1 (when using EXT\_REF)

ADC gain coefficient for user selecting Config1 register EXT\_REF bit as reference. We provide a default value and user is responsible for writing proper value to the register if they want to compensate external reference error. This register does not take effect when EXT\_REF = 0 and internal reference is selected.

**Table 17. GN\_Trim1 Format**

Bit	15	14	13	12	11	10	9	8
Description	N/A	N/A	N/A	N/A	N/A	GN10	GN9	GN8
Default Value	0	0	0	0	0	0	1	1
Bit	7	6	5	4	3	2	1	0
Description	GN7	GN6	GN5	GN4	GN3	GN2	GN1	GN0
Default Value	1	1	1	1	1	0	1	0

ADC GN\_Trim1 register is an unsigned value. Default value used for final trimming is 1.3333 to compensate default ADC gain of 3/4. The value of GN[10:0] adds a constant to get the final gain trimming value.

$GN\_Trim1 + CONST = GN\_Trim$ . The binary value of CONST is 1010011010110000, corresponding to a gain factor of 1.30225. After adding the default value of GN\_Trim1 register (01111111010), the final default gain trimming value is 1.3333. The MAX final gain trimming value is 1.3547 when trimming register is all '1'; MIN value is 1.30225 when register is all '0'. This gives GN trimming a  $\pm 3\%$  range and 32ppmFS step.

## APPLICATION INFORMATION

The following sections give example circuits and suggestions for using the SGM58031 in various situations.

## Basic Connections

For many applications, connecting the SGM58031 is simple. A basic connection diagram for the SGM58031 is shown in Figure 12.

The fully differential voltage input of the SGM58031 is ideal for connection to differential sources with moderately low source impedance, such as thermocouples and thermistors. Although the SGM58031 can read bipolar differential signals, they cannot accept negative voltages on either input. It may be helpful to think of the SGM58031 positive voltage input as non-inverting, and of the negative input as inverting.

When the SGM58031 is converting data, it draws current in short spikes. The 0.1µF bypass capacitor supplies the momentary bursts of extra current needed from the supply.

The SGM58031 interfaces directly to standard mode, fast mode, and high-speed mode I<sup>2</sup>C controllers. Any microcontroller I<sup>2</sup>C peripheral, including master-only and non-multiple-master I<sup>2</sup>C peripherals, can operate with the SGM58031. The SGM58031 does not perform clock-stretching (that is, it never pulls the clock line low),

so it is not necessary to provide for this function unless other clock-stretching devices are on the same I<sup>2</sup>C bus.

Pull-up resistors are required on both the SDA and SCL lines because I<sup>2</sup>C bus drivers are open-drain. The size of these resistors depends on the bus operating speed and capacitance of the bus lines. Higher-value resistors consume less power, but increase the transition times on the bus, limiting the bus speed. Lower-value resistors allow higher speed at the expense of higher power consumption. Long bus lines have higher capacitance and require smaller pull-up resistors to compensate. The resistor value should not be too small; if they are small, the bus drivers may not be able to pull the bus lines low.

## Connecting Multiple Devices

Connecting multiple SGM58031s to a single bus is simple. Using the address pin, the SGM58031 can be set to one of four different I<sup>2</sup>C addresses. An example showing three SGM58031 devices is given in Figure 13. Up to four SGM58031s (using different address pin configurations) can be connected to a single bus.

Note that only one set of pull-up resistors is needed per bus. The pull-up resistor values may need to be lowered slightly to compensate for the additional bus capacitance presented by multiple devices and increased line length.

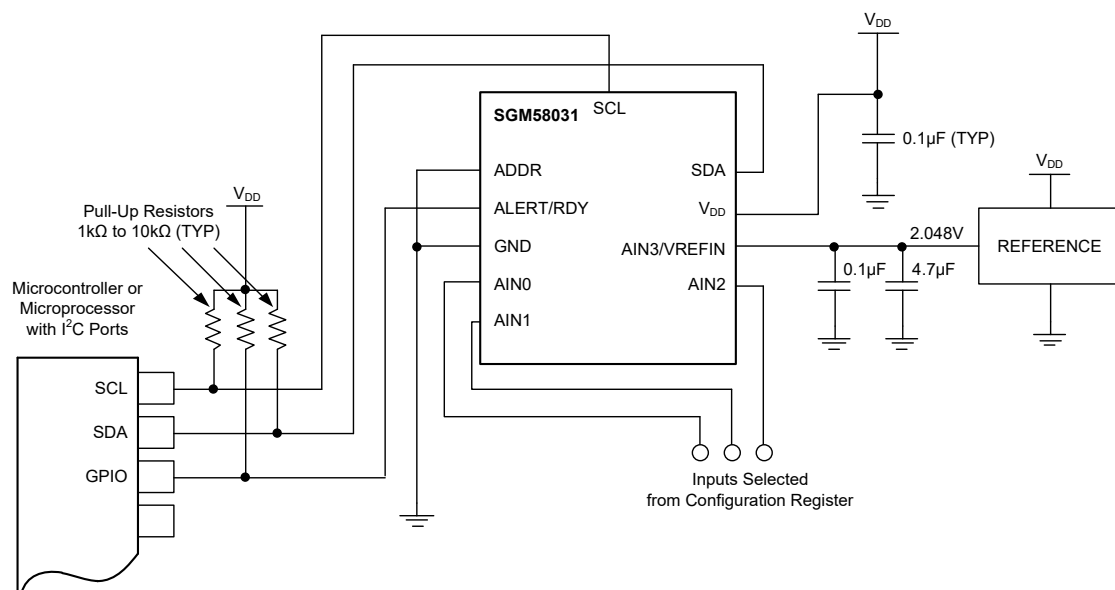
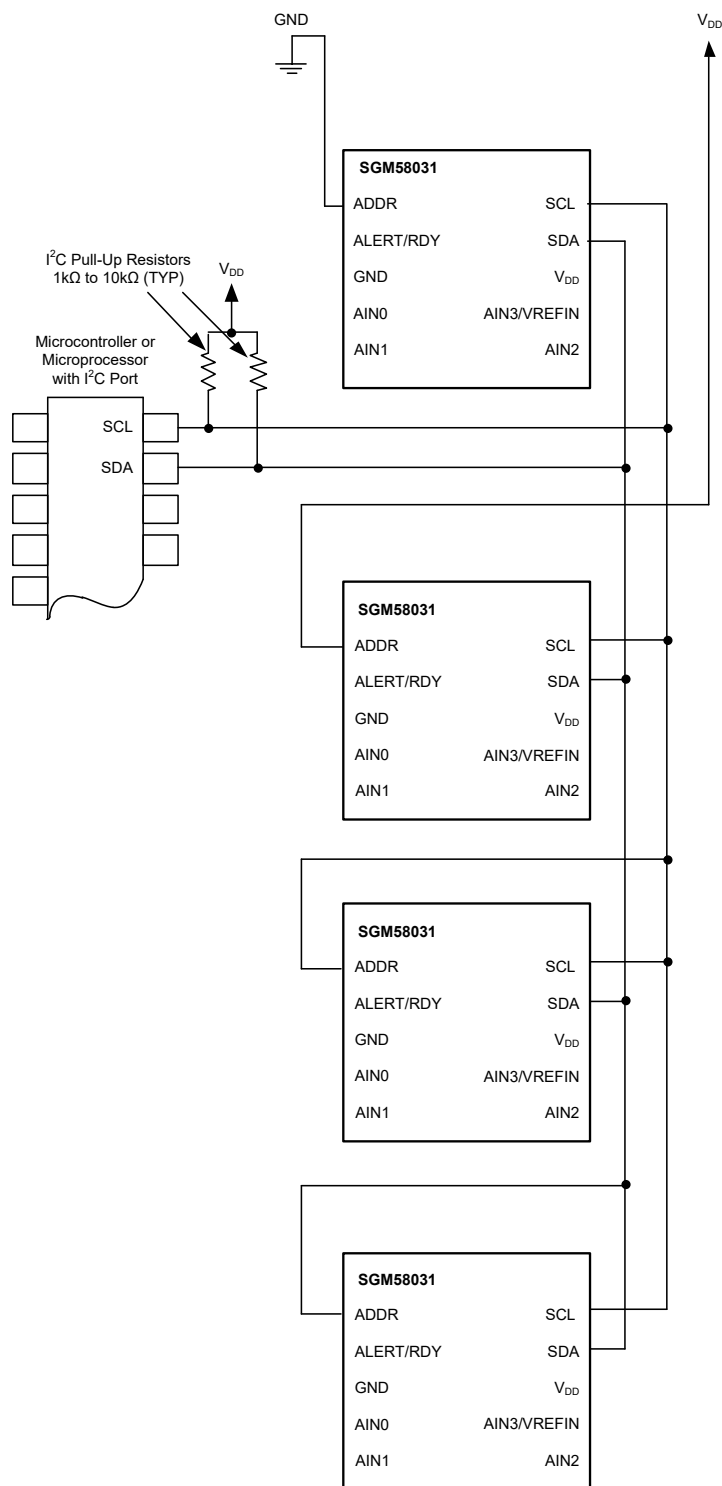


Figure 12. Typical Connections of the SGM58031

## APPLICATION INFORMATION (continued)



NOTE: SGM58031 power and input connections omitted for clarity. The ADDR pin selects the I<sup>2</sup>C address.

**Figure 13. Connecting Multiple SGM58031s**

**APPLICATION INFORMATION (continued)****Using GPIO Ports for Communication**

Most microcontrollers have programmable input/output (I/O) pins that can be set in software to act as inputs or outputs. If an I<sup>2</sup>C controller is not available, the SGM58031 can be connected to GPIO pins and the I<sup>2</sup>C bus protocol is simulated, or bit-banged, in software. An example of this configuration for a single SGM58031 is shown in Figure 14.

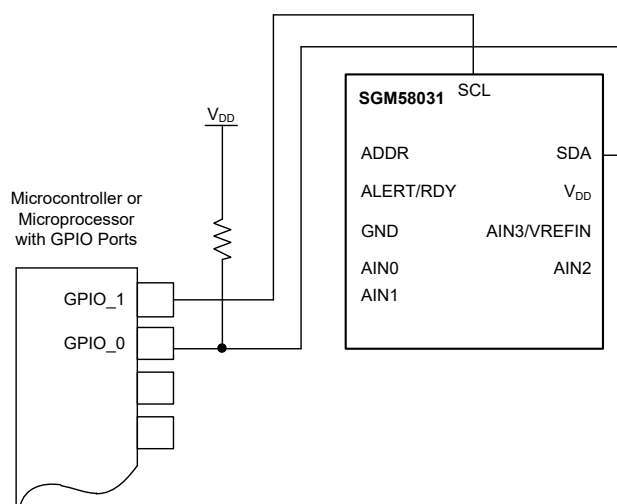
Bit-banging I<sup>2</sup>C with GPIO pins can be done by setting the GPIO line to '0' and toggling it between input and output modes to apply the proper bus states. To drive the line low, the pin is set to output '0'; to let the line go high, the pin is set to input. When the pin is set to input, the state of the pin can be read; if another device is pulling the line low, this configuration reads as a '0' in the port input register.

Note that no pull-up resistor is shown on the SCL line. In this simple case, the resistor is not needed; the

microcontroller can simply leave the line on output, and set it to '1' or '0' as appropriate. This action is possible because the SGM58031 never drives the clock line low. This technique can also be used with multiple devices, and has the advantage of lower current consumption as a result of the absence of a resistive pull-up.

If there are any devices on the bus that may drive the clock lines low, this method should not be used; the SCL line should be high-Z or '0' and a pull-up resistor should be provided as usual.

Some microcontrollers have selectable strong pull-up circuits built in to the GPIO ports. In some cases, these circuits can be switched on and used in place of an external pull-up resistor. Weak pull-ups are also provided on some microcontrollers, but usually these are too weak for I<sup>2</sup>C communication. If there is any doubt about the matter, test the circuit before committing it to production.



NOTE: SGM58031 power and input connections omitted for clarity.

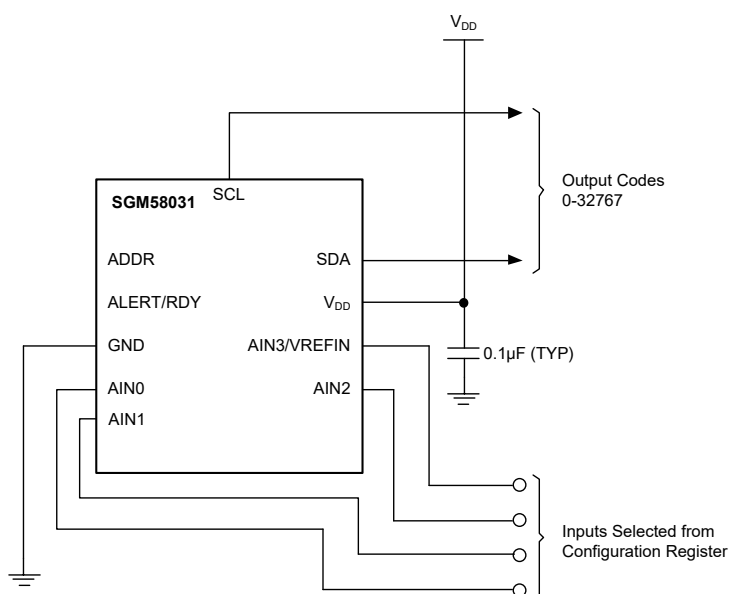
**Figure 14. Using GPIO with a Single SGM58031**

**APPLICATION INFORMATION (continued)****Single-Ended Inputs**

Although the SGM58031 has two differential inputs, the device can easily measure four single-ended signals. Figure 15 shows a single-ended connection scheme. The SGM58031 is configured for single-ended measurement by configuring the MUX to measure each channel with respect to ground. Data are then read out of one input based on the selection on the configuration register. The single-ended signal can range from 0V to supply. The SGM58031 loses no linearity anywhere

within the input range. Negative voltages cannot be applied to this circuit because the SGM58031 can only accept positive voltages.

The SGM58031 input range is bipolar differential with respect to the reference. The single-ended circuit shown in Figure 15 covers only half the SGM58031 input scale because it does not produce differentially negative inputs; therefore, one bit of resolution is lost.



NOTE: Digital and address pin connections omitted for clarity.

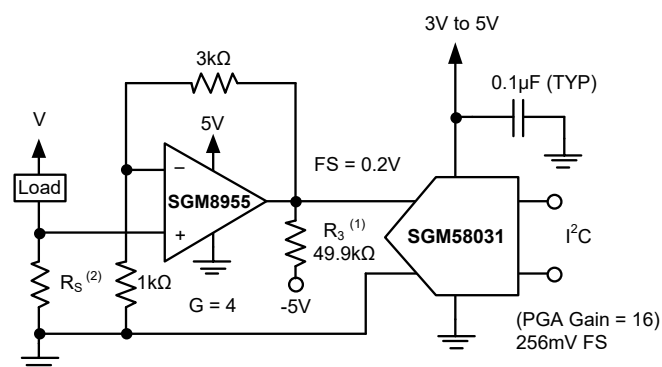
**Figure 15. Measuring Single-Ended Inputs**

## APPLICATION INFORMATION (continued)

## Low-Side Current Monitor

Figure 16 shows a circuit for a low-side shunt-type current monitor. The circuit monitors the voltage across a shunt resistor, which is sized as small as possible while giving a measurable output voltage. This voltage is amplified by an SGM8955 low-drift op amp, and the result is read by the SGM58031.

It is suggested that the SGM58031 be operated at a gain of 8. The gain of the SGM8955 can then be set lower. For a gain of 16, the op amp should be set up to give a maximum output voltage no greater than 0.256V. If the shunt resistor is sized to provide a maximum voltage drop of 50mV at full-scale current, the full-scale input to the SGM58031 is 0.2V.



## NOTES:

1. Pull-down resistor to allow accurate swing to 0V.
2.  $R_S$  is sized for a 50mV drop at full-scale current.

Figure 16. Low-Side Current Measurement

The SGM58031 is fabricated in a small-geometry, low-voltage process. The analog inputs feature protection diodes to the supply rails. However, the current-handling ability of these diodes is limited, and the SGM58031 can be permanently damaged by analog input voltages that remain more than approximately 300mV beyond the rails for extended periods. One way to protect against overvoltage is to place current-limiting resistors on the input lines. The SGM58031 analog inputs can withstand momentary currents as large as 100mA.

If the SGM58031 is driven by an op amp with high-voltage supplies, such as  $\pm 12V$ , protection should be provided, even if the op amp is configured so that it does not output out-of-range voltages. Many op amps drift to one of the supply rails immediately when power is applied, usually before the input has stabilized; this momentary spike can damage the SGM58031. This incremental damage results in slow, long-term failure, which can be disastrous for permanently installed, low-maintenance systems.

If an op amp or other front-end circuitry is used with a SGM58031, performance characteristics must be taken into account when designing the application.

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

## MARCH 2020 – REV.A to REV.A.1

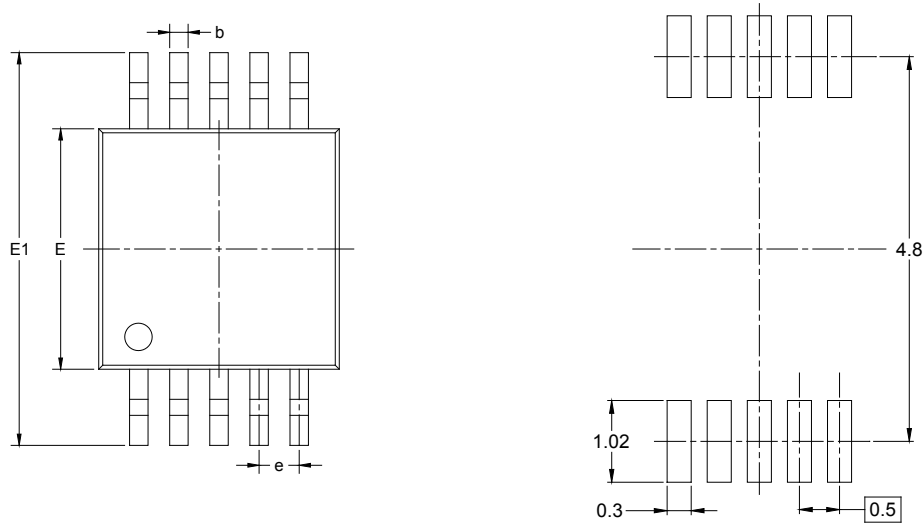
	Page
Update Figure 4 and Figure 5 .....	12

## Changes from Original (DECEMBER 2019) to REV.A

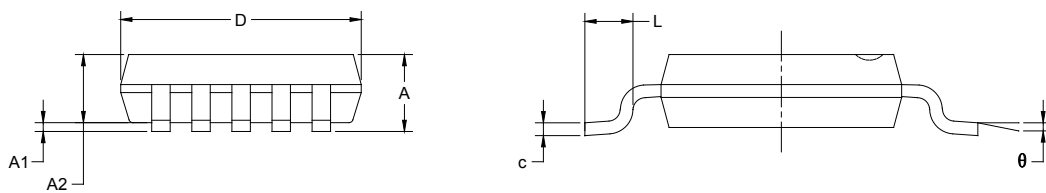
	Page
Changed from product preview to production data .....	All

## PACKAGE OUTLINE DIMENSIONS

### MSOP-10



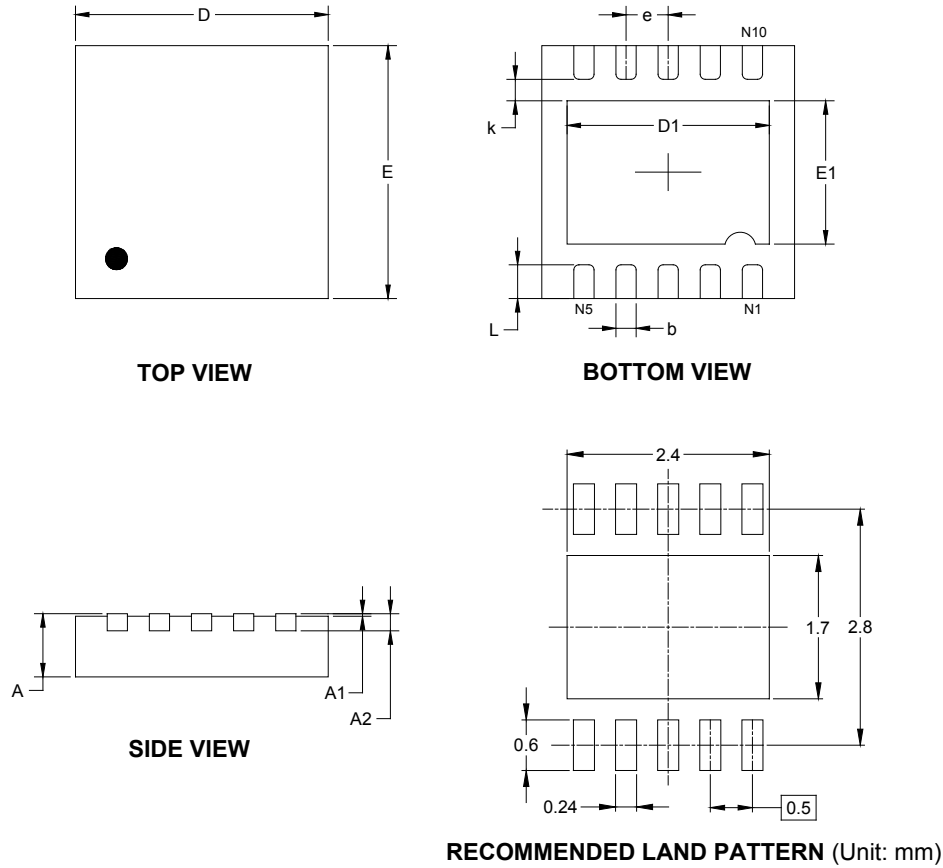
RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.500 BSC		0.020 BSC	
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

## PACKAGE OUTLINE DIMENSIONS

### TDFN-3×3-10L



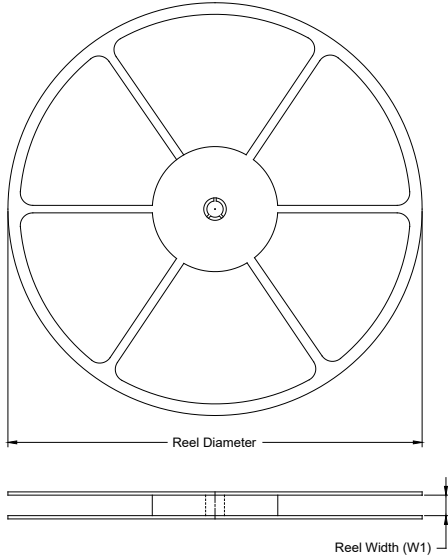
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.103
E	2.900	3.100	0.114	0.122
E1	1.500	1.800	0.059	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020



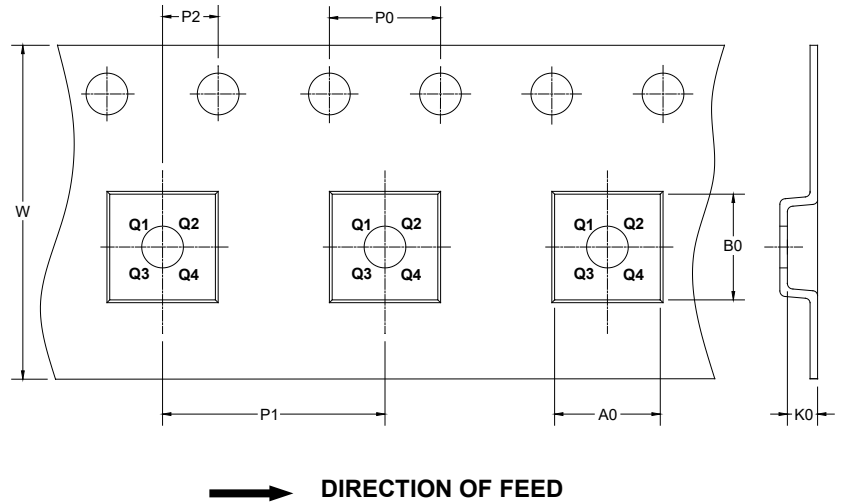
## PACKAGE INFORMATION

### TAPE AND REEL INFORMATION

#### REEL DIMENSIONS



#### TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

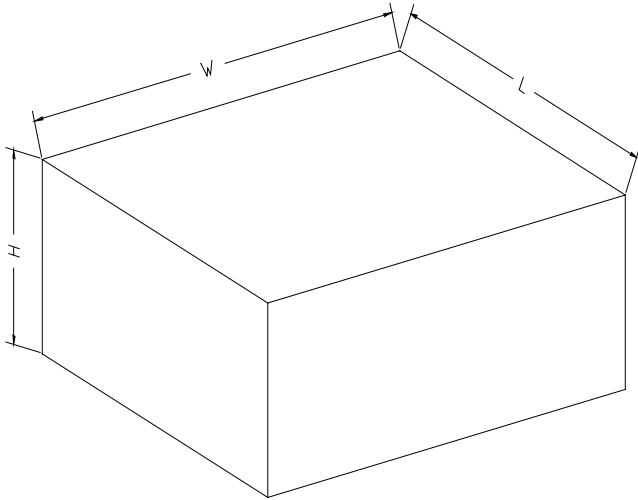
#### KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
MSOP-10	13"	12.4	5.20	3.30	1.20	4.0	8.0	2.0	12.0	Q1
TDFN-3×3-10L	13"	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q1

DD0001

## PACKAGE INFORMATION

### CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

### KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5

DD0002